



2000V / 45mOhm SiC MOSFET - Bare Die

HWDS2Q200045BD

Product Overview

The HWDS2Q200045BD is a high-voltage 2nd Generation silicon carbide MOSFET supplied in bare die form, designed for high-efficiency, high-frequency power conversion. Its 2000V blocking voltage, low on-resistance, robust intrinsic body diode, and 175°C junction temperature capability support demanding industrial, solar, and power-supply applications.

Features

- 2nd Generation SiC MOSFET Technology with +15~+18V gate drive
- High blocking voltage with low on-resistance
- High speed switching with low capacitance
- 175°C operating junction temperature capability
- Very fast and robust intrinsic body diode
- Kelvin gate input easing driver circuit design
- Bare die format: suitable for custom packaging and direct die attach

Applications

- Solar boosters
- UPS power supplies
- Motor drivers
- Switch mode power supplies
- High voltage DC-DC converters

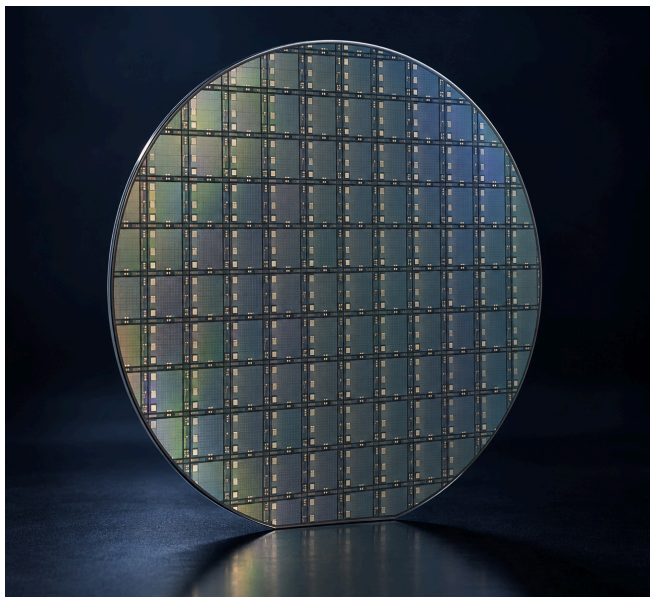
Part Number Information

Part Number	Description	Package
HWDS2Q200045BD	2000V 45mΩ SiC MOSFET Bare Die	Die (BD suffix)



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$T_C=25^{\circ}\text{C}$ unless otherwise specified

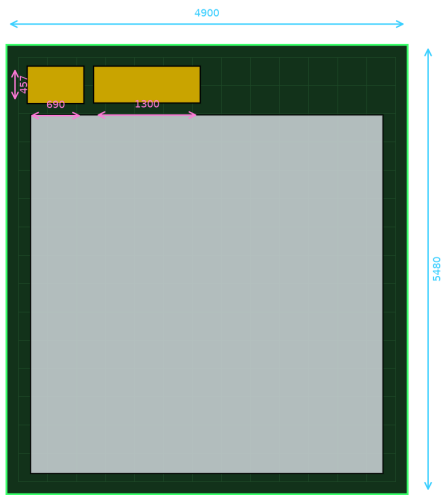
Symbol	Parameter	Value	Unit	Test Conditions	Note
Vds	Drain-Source voltage	2000	V	Vgs=0V, Id=100μA	
Vgsmax (Transient)	Maximum transient voltage	-10 to 23	V	Duty cycle<1%, and pulse width<200ns	
Vgson	Recommended turn-on voltage	15 to 18	V		
Vgsoff	Recommended turn-off voltage	-5 to -2	V	Typical -3.5V	
Id	Drain current (continuous)	62	A	Vgs=18V, Tc=25°C	Fig.23
Idc	Drain current (continuous)	46	A	Vgs=18V, Tc=100°C	Fig.23
Idm	Drain current (pulsed)	155	A	Pulse width limited by SOA and dynamic Rθ(j-c)	Fig.25,26
Ism	Body diode current (pulsed)	155	A	Pulse width limited by SOA and dynamic Rθ(j-c)	Fig.25,26
Ptot	Total power dissipation	500	W	Tc=25°C	Fig.24
Tstg	Storage temperature range	-55 to 175	°C		
Tj	Operating junction temperature	-55 to 175	°C		
Tl	Solder Temperature	260	°C	Wave soldering only allowed at leads, 1.6mm from case for 10s	

Note 1: Assumes Rθ(j-c) < 0.3°C/W.



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Chip size (W/O scribe line): 4900×5480μm

Chip size (With scribe line): 4980×5560μm

Gate Pad: 690×457μm

Kelvin Source Pad: 1300×450μm

*Die outline dimensions are engineering estimates; contact

sales for confirmed die-level metrology on a per-lot basis.

Mechanical Parameters

Parameter	Typ.	Unit
Die Size	4900 × 5480	μm ²
Source Pad Size (L×W)	3900 × 4400	μm ²
Kelvin Pad Size (L×W)	1300 × 450	μm ²
Gate Pad Size (L×W)	690 × 457	μm ²
Thickness	180 ± 20	μm
Wafer Size	150	mm
Top Side Source Metallization (AlCu)	4	μm
Top Side Gate Metallization (AlCu)	4	μm
Bottom Drain Metallization (Ti/Ni/Ag)	0.2 / 0.2 / 1	μm
Frontside Passivation (Polyimide)	5	μm

*Mechanical parameter values above are representative engineering estimates based on the device electrical rating class; the source specification did not publish die-level mechanical data for this part.



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Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	Note
Idss	Zero gate voltage drain current		1	10	μA	$V_{ds}=2000\text{V}$, $V_{gs}=0\text{V}$	
Igss	Gate leakage current			± 100	nA	$V_{ds}=0\text{V}$, $V_{gs}=-5\sim 20\text{V}$	
Vth	Gate threshold voltage	1.8	2.8	4.5	V	$V_{gs}=V_{ds}$, $I_d=10\text{mA}$	Fig.8,9
Vth	Gate threshold voltage		2.2		V	$V_{gs}=V_{ds}$, $I_d=10\text{mA}$ @ $T_j=175^{\circ}\text{C}$	
Ron	Static drain-source on-resistance		43	56	m Ω	$V_{GS}=18\text{V}$, $I_D=20\text{A}$ @ $T_j=25^{\circ}\text{C}$	Fig.4,5,6,7
Ron	Static drain-source on-resistance		105		m Ω	$V_{gs}=18\text{V}$, $I_d=20\text{A}$ @ $T_j=175^{\circ}\text{C}$	
Ron	Static drain-source on-resistance		48		m Ω	$V_{gs}=15\text{V}$, $I_d=20\text{A}$ @ $T_j=25^{\circ}\text{C}$	
Ron	Static drain-source on-resistance		110		m Ω	$V_{gs}=15\text{V}$, $I_d=20\text{A}$ @ $T_j=175^{\circ}\text{C}$	
Ciss	Input capacitance		3950		pF	$V_{ds}=1500\text{V}$, $V_{gs}=0\text{V}$, $f=1\text{MHz}$	Fig.16
Coss	Output capacitance		110		pF		
Crss	Reverse transfer capacitance		13		pF		
Eoss	Coss stored energy		145		μJ		Fig.17
Qg	Total gate charge		175		nC	$V_{ds}=1500\text{V}$, $I_d=20\text{A}$, $V_{gs}=-3$ to 18V	Fig.18
Qgs	Gate-source charge		43		nC		
Qgd	Gate-drain charge		63		nC		
Rg	Gate input resistance		1.5		Ω	$f=1\text{MHz}$	
Eon	Turn-on switching energy		870		μJ	$V_{ds}=1200\text{V}$, $I_d=20\text{A}$, $V_{gs}=-3.5$ to 18V , $R_{g(\text{ext})}=3.3\Omega$, $L=400\mu\text{H}$, $T_j=25^{\circ}\text{C}$	Fig.19,20
Eoff	Turn-off switching energy		150		μJ		
td(on)	Turn-on delay time		25		ns		
tr	Rise time		24		ns		
td(off)	Turn-off delay time		40		ns		
tf	Fall time		23		ns		

Reverse Diode Characteristics

$T_C=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	Note
Vsd	Diode forward voltage		3.5		V	$I_{sd}=20\text{A}$, $V_{gs}=0\text{V}$	Fig.10,11,12
Vsd	Diode forward voltage		3.4		V	$I_{sd}=20\text{A}$, $V_{gs}=0\text{V}$, $T_j=175^{\circ}\text{C}$	
trr	Reverse recovery time		46		ns	$V_{gs}=-3.5\text{V}/+18\text{V}$, $I_{sd}=20\text{A}$, $V_r=1200\text{V}$, $R_{g(\text{ext})}=5.1\Omega$, $di/dt=3000\text{A}/\mu\text{s}$	
Qrr	Reverse recovery charge		550		nC		
Irrm	Peak reverse recovery current		23		A		



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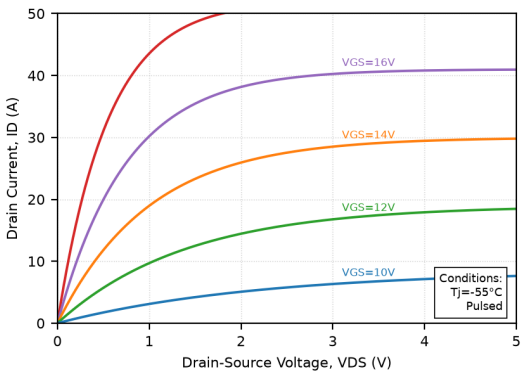


Fig. 1 — Output Curve @ Tj=-55°C

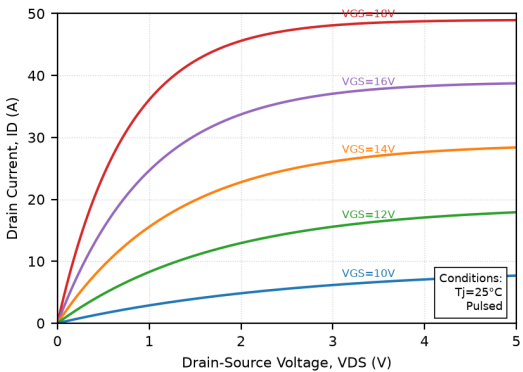


Fig. 2 — Output Curve @ Tj=25°C

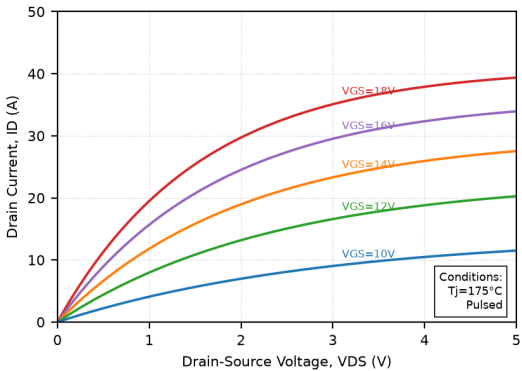


Fig. 3 — Output Curve @ Tj=175°C

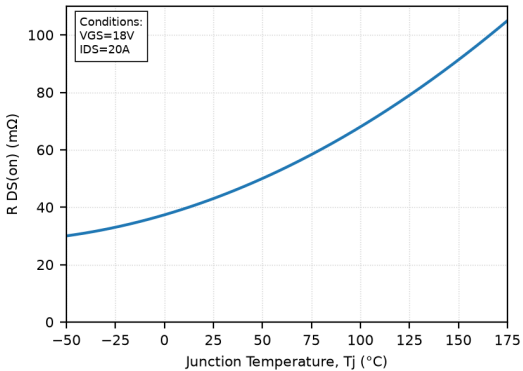


Fig. 4 — R DS(on) vs. Junction Temperature



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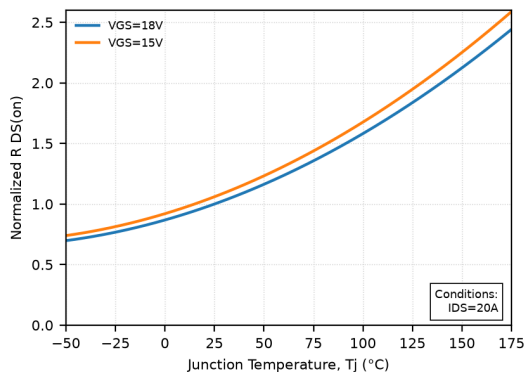


Fig. 5 — Normalized $R_{DS(on)}$ vs. Junction Temp

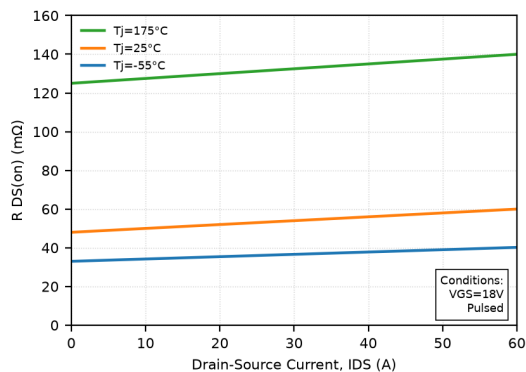


Fig. 6 — $R_{DS(on)}$ vs. I_{DS} @ Various Temperature

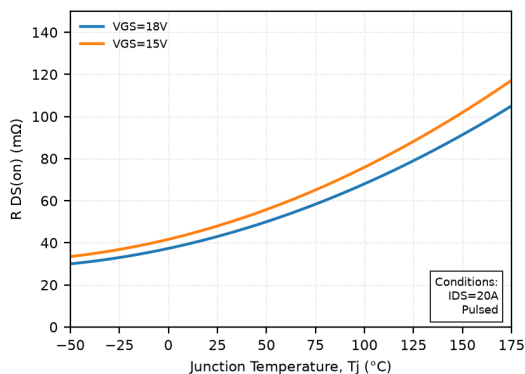


Fig. 7 — $R_{DS(on)}$ vs. Temperature @ Various V_{GS}

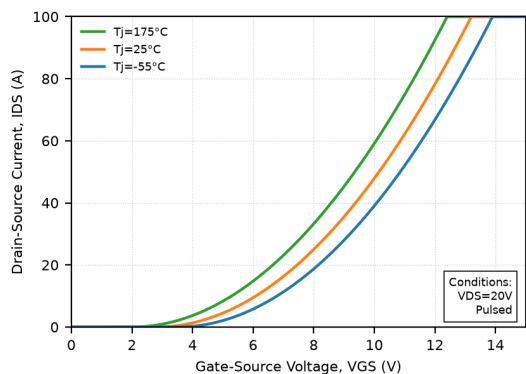


Fig. 8 — Transfer Curves @ Various Temperature



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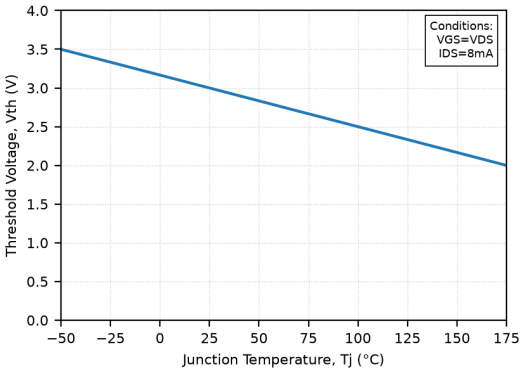


Fig. 9 — V_{th} vs. Junction Temperature

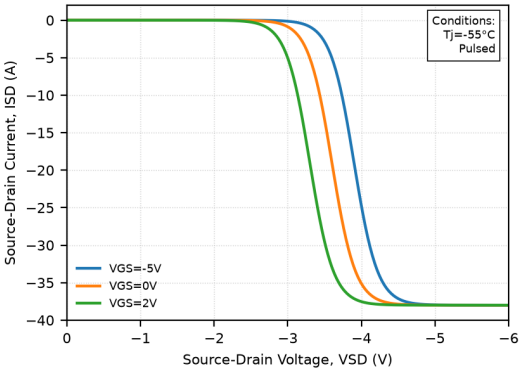


Fig. 10 — Body Diode I-V @ $T_j = -55^{\circ}C$

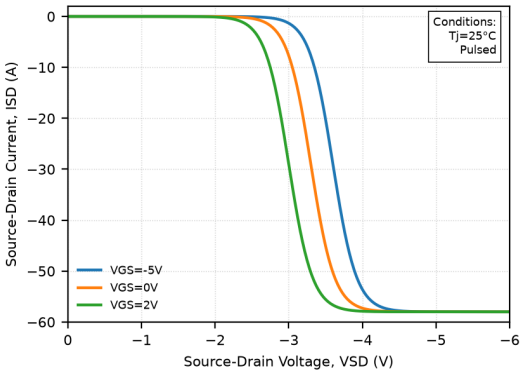


Fig. 11 — Body Diode I-V @ $T_j = 25^{\circ}C$

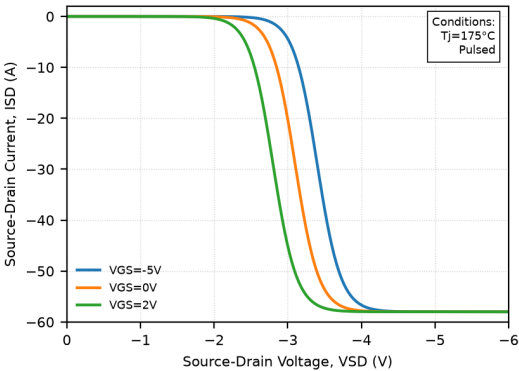


Fig. 12 — Body Diode I-V @ $T_j = 175^{\circ}C$