



H3M065F011

Silicon Carbide MOSFET
N-CHANNEL ENHANCEMENT MODE

Features

- Low On-Resistance and High Current Density
- Low Capacitance for High Frequency Operation
- Positive Temperature Coefficient Device
- RoHS Compliant and Halogen Free

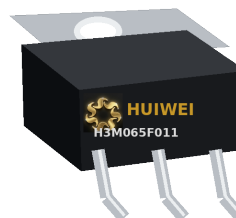
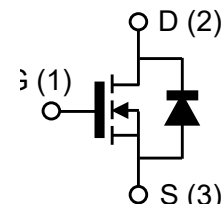
Benefits

- Higher System Efficiency
- Increase Parallel Device Convenience
- Capable of 175°C High T_j Application
- Allow High Frequency Operation
- Realize Compact and Lightweight Systems

Applications

- Switching Mode Power Supply
- DC/DC Converters, UPS, and PFC
- Power Inverters
- Auxiliary Power Supplies
- Solar/Wind Renewable Energy

V_{DS}	650V
$I_D(@25^{\circ}C)$	194A
$R_{DS(on)}$	11mΩ



		Marking
H3M065F011	TO-247-3L	H3M065F011

Description

The H3M065F011 650V, 11mΩ silicon carbide power MOSFET is an N-channel enhancement mode device. Exploiting the outstanding wide bandgap material properties, this device shows high current density and great switching behavior. Thanks for the excellent thermal conductivity and many advantages of SiC, this device significantly improved in thermal capability and temperature independent switching behavior.

Absolute Maximum Ratings ($T_c = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Value	Unit
Drain – Source Voltage	$V_{DS, max}$	$V_{GS}=0V, I_D=100\mu A$	650	V
Continuous Drain Current	I_D	$V_{GS}=18V, T_c=25^{\circ}C$	194	A
		$V_{GS}=18V, T_c=110^{\circ}C$	130	
Pulse Drain Current	$I_{D, pulse}$	t_{PW} limitation per Fig.17	622	
Avalanche energy, Single Pulse	E_{AS}	$V_{DD}=100V, I_D=42.5A, L=5mH$	4516	mJ
Power Dissipation	P_D	$T_c=25^{\circ}C$	517	W
Recommend Gate Source Voltage	$V_{GS, op}$	Static, recommended DC operating values	-5 to 18	V
Maximum Gate Source Voltage	$V_{GS, max}$	Transient operating limit (AC $f > 1Hz$, duty cycle $< 1\%$)	-10 to 25	
Junction & Storage Temperature	T_j, T_{stg}		-55 to 175	$^{\circ}C$
Soldering Temperature	T_L		260	
Mounting Torque	M_D	M3 or 6-32 screw	1.0	Nm

Thermal Resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal Resistance, Junction to Case	$R_{\theta, JC}$		0.29		$^{\circ}C/W$

**Electrical Characteristics** ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_{DS}=100\mu A$	650			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_{DS}=28mA$	2	2.8	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=650V, V_{GS}=0V$		<1	50	μA
		$V_{DS}=650V, V_{GS}=0V$ $T_j=175^\circ\text{C}$		1		
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=18V, V_{DS}=0V$			250	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=15V, I_{DS}=100A$		14	19	mΩ
		$V_{GS}=18V, I_{DS}=100A$		11	15	
		$V_{GS}=18V, I_{DS}=100A$, $T_j=175^\circ\text{C}$		12.5		
Transconductance	g_{fs}	$V_{DS}=10V, I_{DS}=100A$		53		S
Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=400V$ $f=1MHz, V_{AC}=25mV$		6220		pF
Output Capacitance	C_{oss}			471		
Reverse Transfer Capacitance	C_{rss}			40		
Effective Output Capacitance, Energy Related	$C_{o(er)}$			615		
Effective Output Capacitance, Time Related	$C_{o(tr)}$	$I_D=const., V_{GS}=0V$, $V_{DS}=0$ to 400V		903		
Turn On Delay Time	$t_{d(on)}$	$V_{DS}=400V, V_{GS}=-3/+18V$, $I_D=100A, L=50\mu H$, $R_{G(ext)}=3.3\Omega$		TBD		ns
Rise Time	t_r			TBD		
Turn Off Delay Time	$t_{d(off)}$			TBD		
Fall Time	t_f			TBD		
C_{oss} Stored Energy	E_{oss}	$V_{GS}=0V, V_{DS}=400V$ $f=1MHz, V_{AC}=25mV$		49		μJ
Turn-on Switching Energy	E_{on}	$V_{DS}=400V, V_{GS}=-3/+18V$, $I_D=100A, L=50\mu H$,		2586		
Turn-off Switching Energy	E_{off}	$R_{G(ext)}=3.3\Omega$		759		
Internal Gate Resistance	$R_{G(int.)}$	$f=1MHz, V_{AC}=25mV$		2.1		Ω

Built-in SiC Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

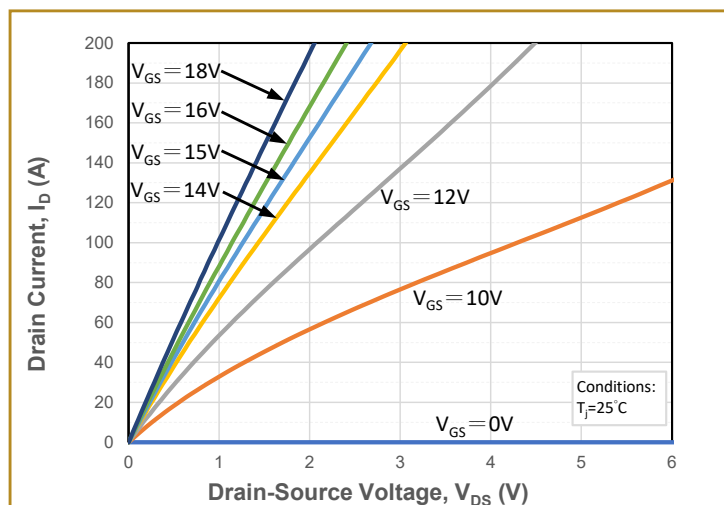
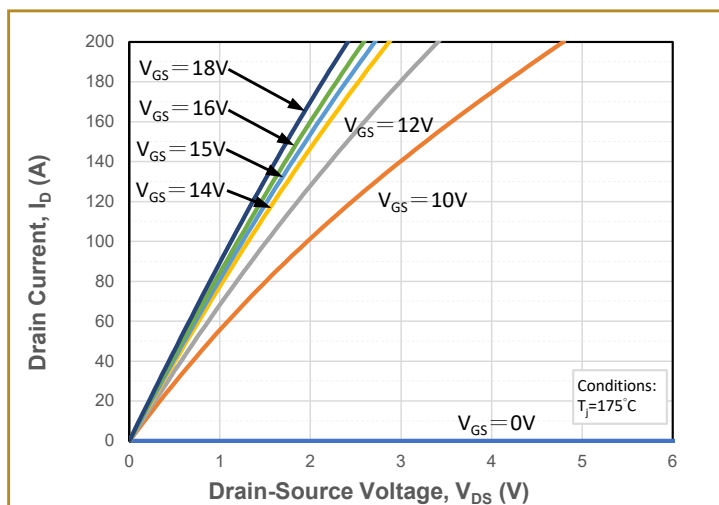
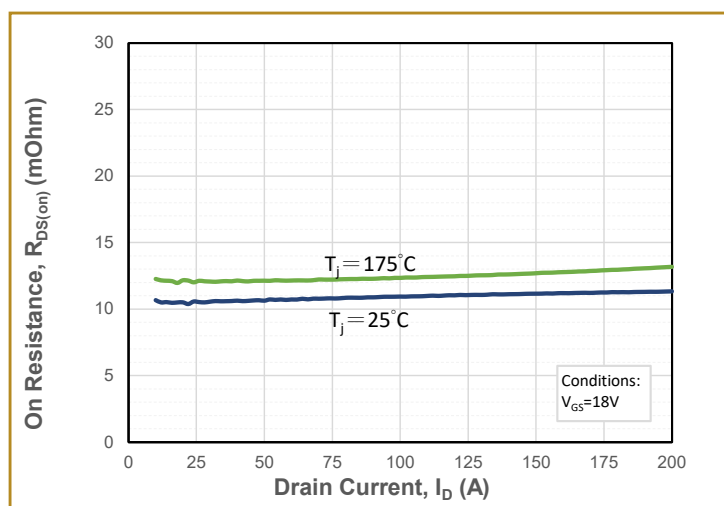
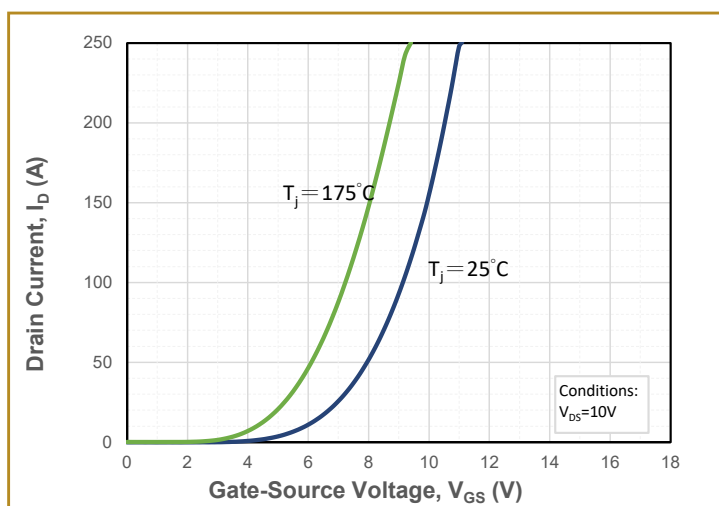
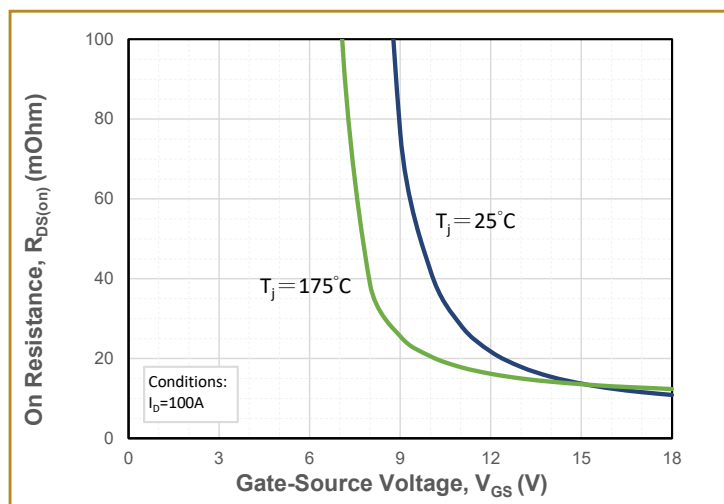
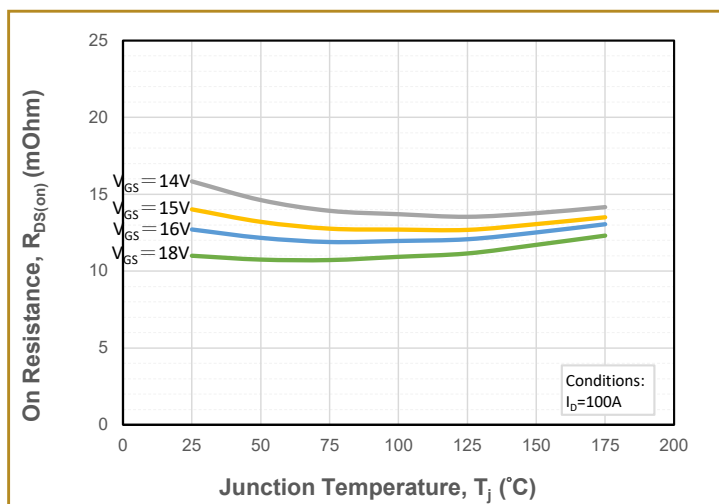
Parameter	Symbol	Test Conditions	Typ.	Unit
Inverse Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_{SD}=50A$	3.3	V
Continuous Diode Forward Current	I_S	$V_{GS}=0V, T_c=25^\circ\text{C}$	194	A
Pulse Diode Forward Current	$I_{S, pulse}$	Pulse width t_{PW} limited by T_{jmax}	622	A
Reverse Recovery Time	t_{rr}	$V_{GS}=-3V$,	TBD	ns
Reverse Recovery Charge	Q_{rr}	$I_{SD}=100A, V_R=400V$,	TBD	nC
Peak Reverse Recovery Current	I_{rrm}	$di/dt=3000A/\mu s$	TBD	A

Gate Charge Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Value	Unit
Gate to Source Charge	Q_{GS}	$V_{DS}=400V$, $V_{GS}=-3/+18V$, $I_D=100A$	68	nC
Gate to Drain Charge	Q_{GD}		82	
Total Gate Charge	Q_G		253	
Gate plateau voltage	V_{pl}		8.4	V



Typical Device Performance

**Fig.1 Forward Output Characteristics at $T_j = 25^\circ C$** **Fig.2 Forward Output Characteristics at $T_j = 175^\circ C$** **Fig.3 On-Resistance vs. Drain Current for Various T_j** **Fig.4 Transfer Characteristics for Various T_j** **Fig.5 On-Resistance vs. Gate Voltage for Various T_j** **Fig.6 On-Resistance vs. Temperature for Various Gate Voltage**



Typical Device Performance

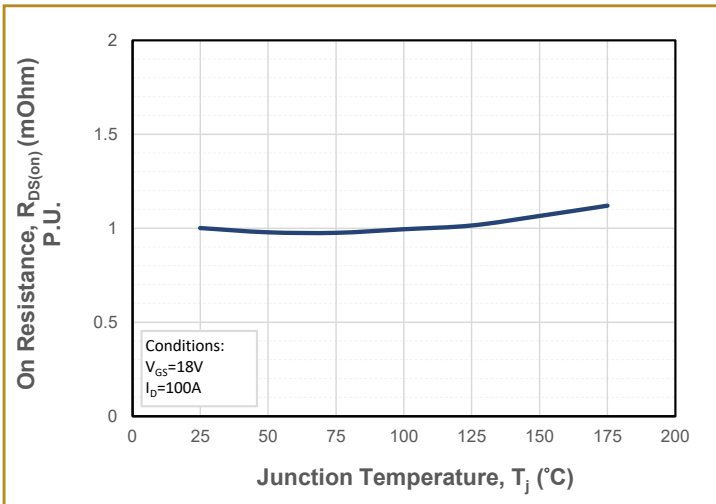


Fig.7 Normalized On-Resistance vs. Temperature

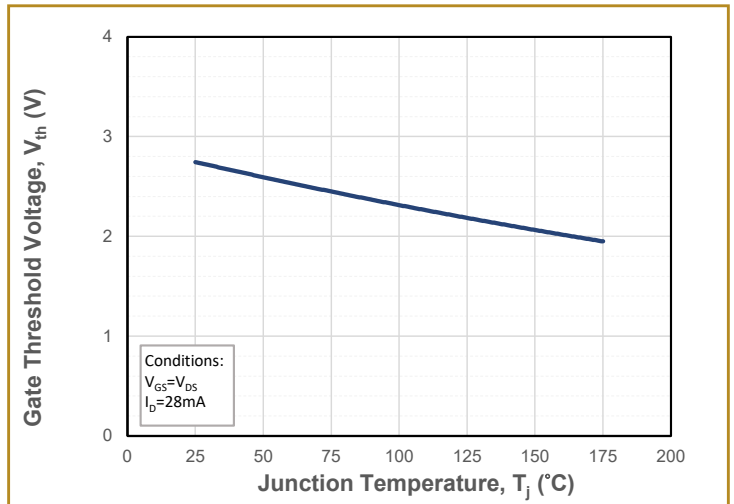


Fig.8 Threshold Voltage vs. Temperature

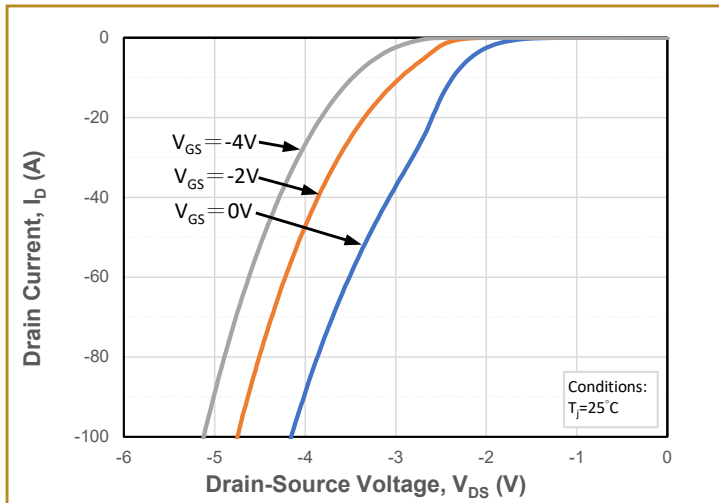


Fig.9 Body Diode Characteristics at $T_j = 25^\circ C$

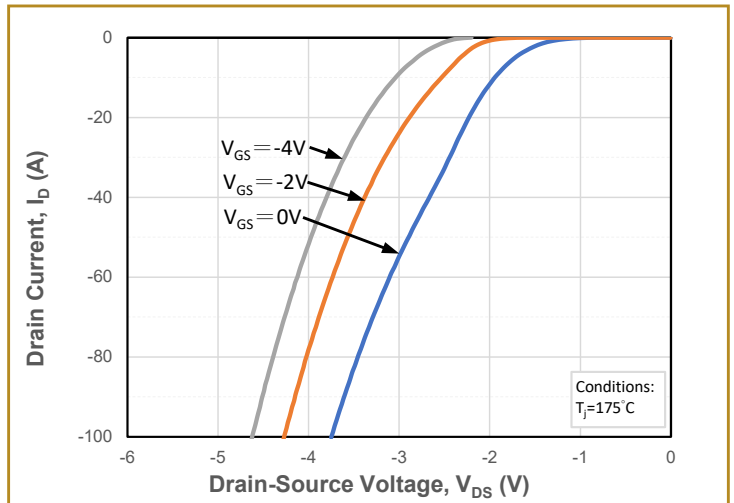


Fig.10 Body Diode Characteristics at $T_j = 175^\circ C$

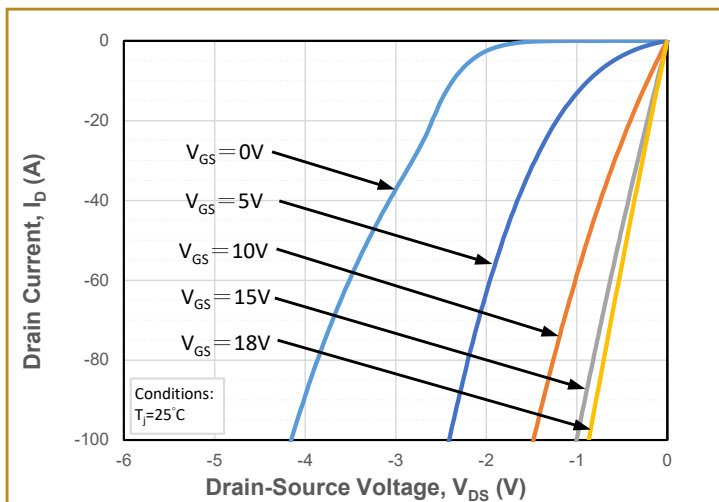


Fig.11 3rd Quadrant Characteristics at $T_j = 25^\circ C$

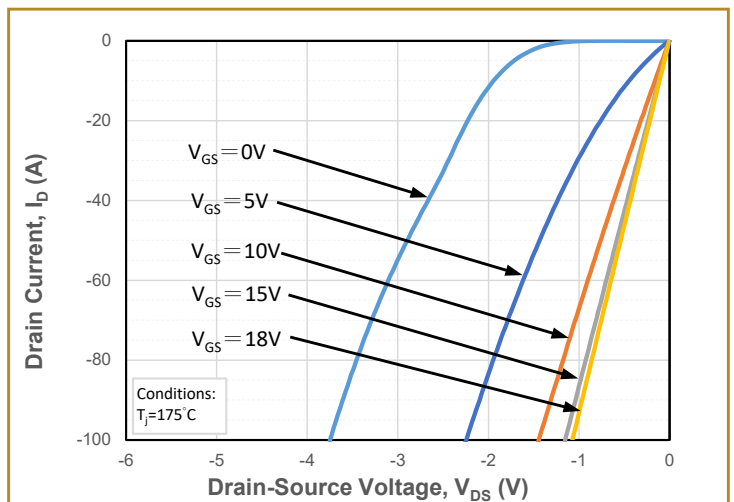


Fig.12 3rd Quadrant Characteristics at $T_j = 175^\circ C$



Typical Device Performance

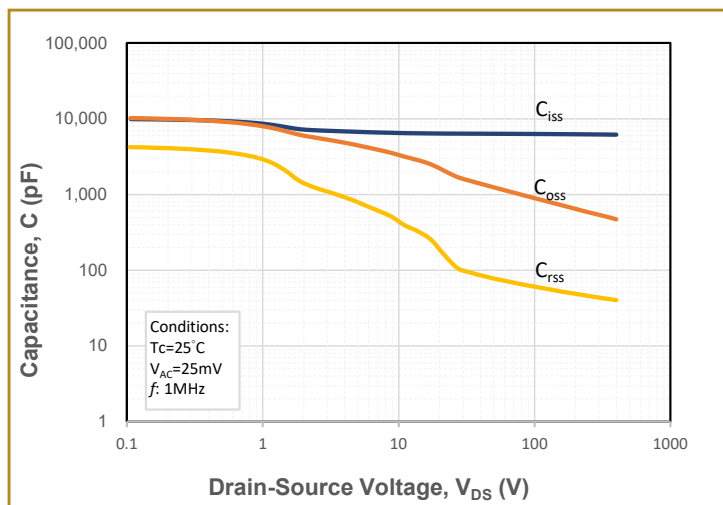


Fig.13 Capacitances vs. Drain to Source Voltage

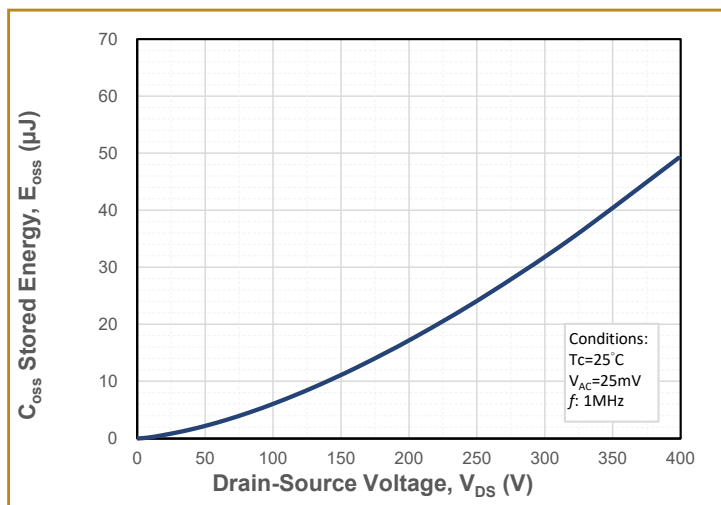


Fig.14 Output Capacitor Stored Energy

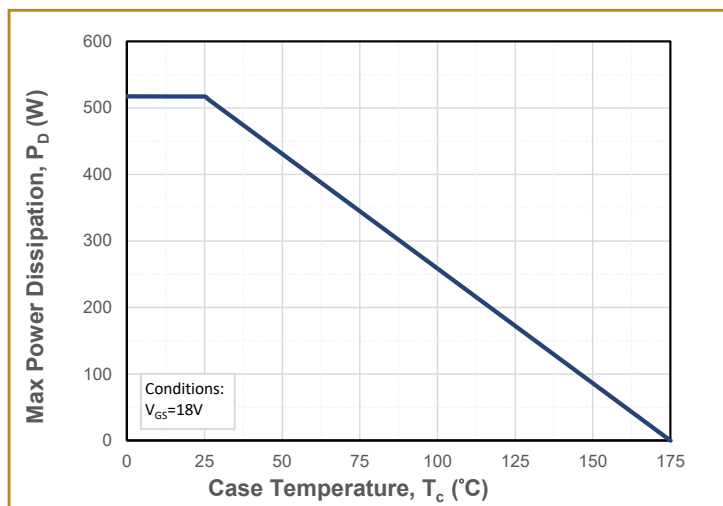


Fig.15 Maximum Power Dissipation Derating vs. Case Temperature

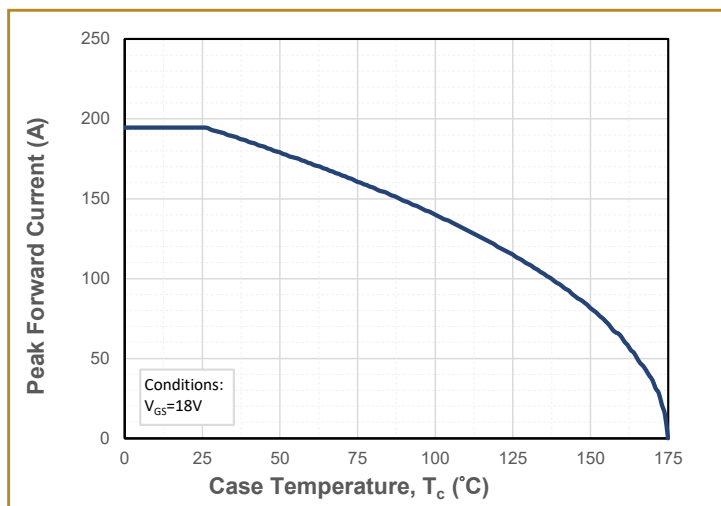


Fig.16 Drain Current Derating vs. Case Temperature

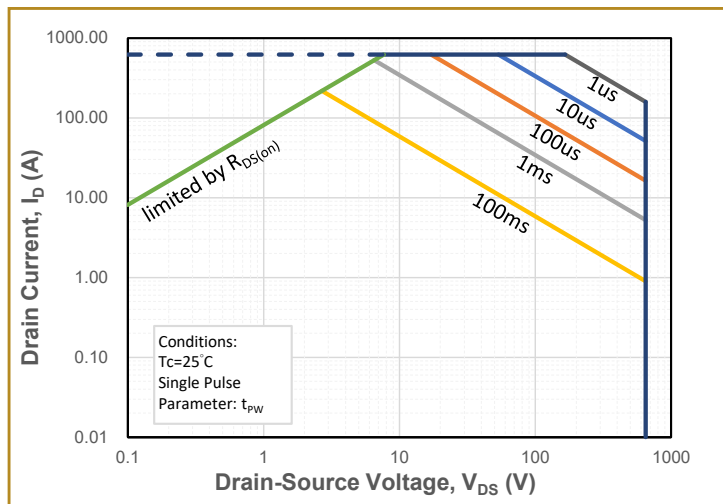


Fig.17 Safe Operating Area

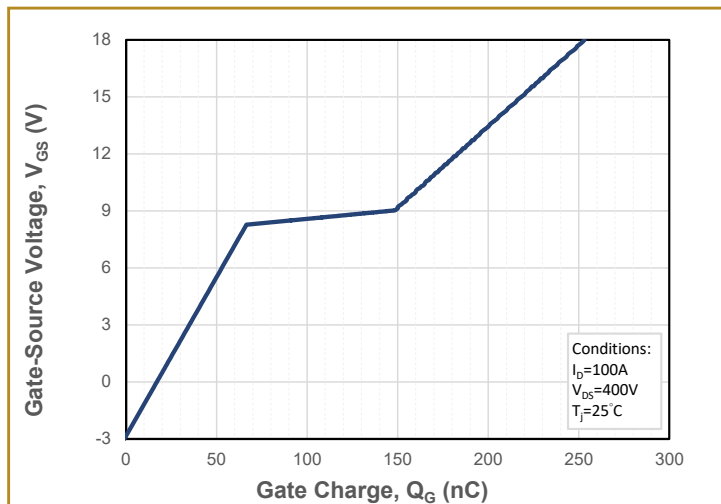


Fig.18 Gate Charge Characteristics



Typical Device Performance

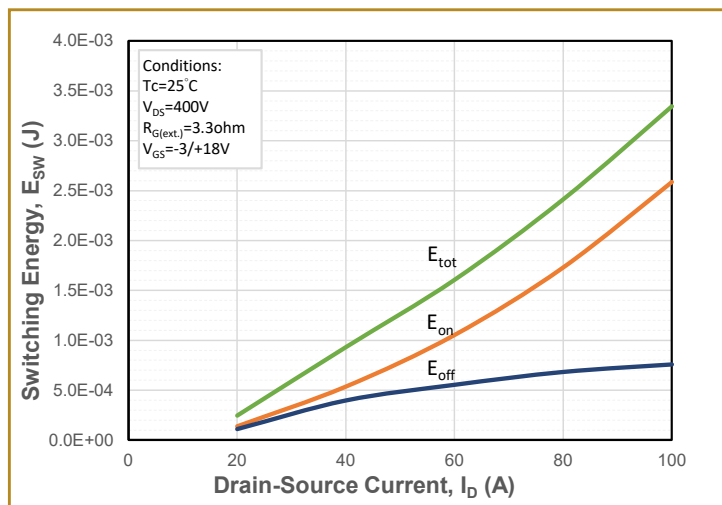


Fig.19 Clamped Inductive Switching Energy vs. Drain Current

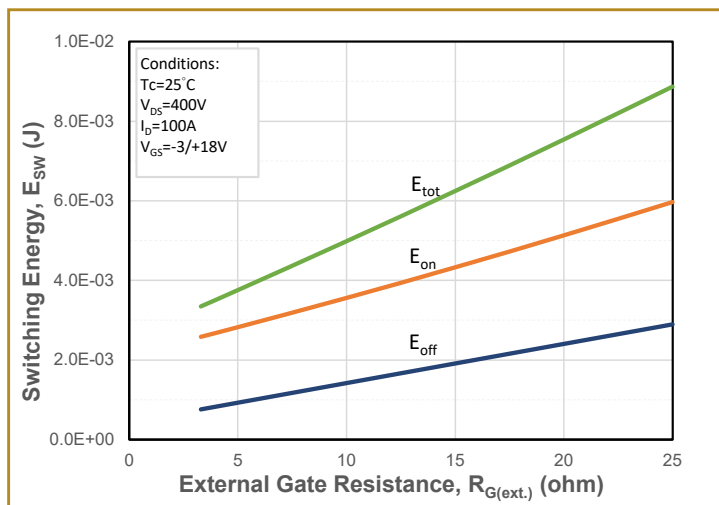


Fig.20 Clamped Inductive Switching Energy vs. External Gate Resistor (R_{G(ext.)})

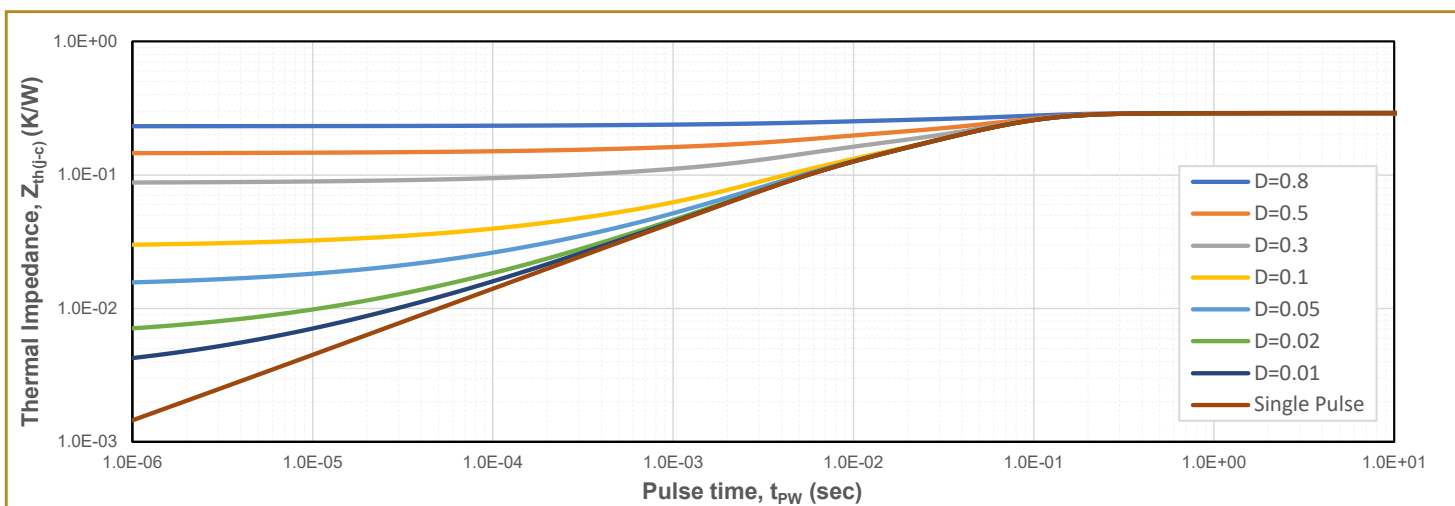


Fig.21 Transient Junction to Case Thermal Impedance

Naming Rule

H3 M 065 F 011

Generation

H3 = 3rd Gen Discrete

Device Type

M = MOSFET J = J MOS

S = JBS diode

Breakdown Voltage

065 = 650V 170 = 1700V

120 = 1200V 330 = 3300V

Package

F = TO-247-3L Q = TO-247-4L

B = TO-220-3L T = TO-263-2L

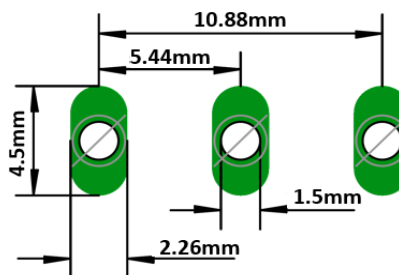
Typical On-Resistance

011 = 11mΩ 016 = 16mΩ 025 = 25mΩ

100 = 100mΩ 220 = 220mΩ

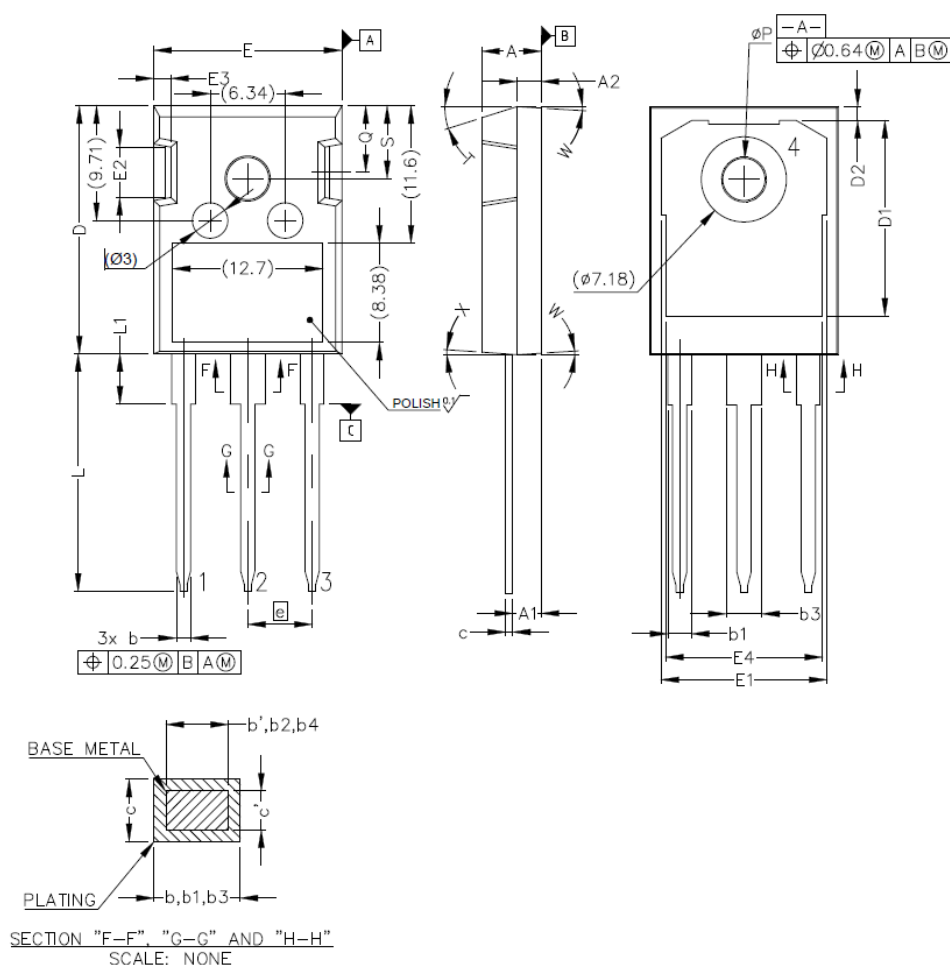
Recommended Solder Pad Layout

TO-247-3L





Package Dimensions



Symbol	mm	
	Min.	Max.
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b'	1.07	1.28
b	1.07	1.33
b1	1.91	2.41
b2	1.91	2.16
b3	2.87	3.38
b4	2.87	3.13
c'	0.55	0.65
c	0.55	0.68
D	20.80	21.10
D1	16.25	17.65
D2	0.95	1.25
E	15.75	16.13
E1	13.10	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
e	5.44 BSC	
N	3	
L	19.81	20.32
L1	4.10	4.40
φP	3.51	3.65
Q	5.49	6.00
S	6.04	6.30
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	

Notes

- The information provided herein is subject to change without notice.
- For other information that does not show on this datasheet, please contact us for inquiry.