HWD70H2DC210A

RoHS COMPLIANT | Pb Pb-Free | HSF HALOGEN FREE

Description

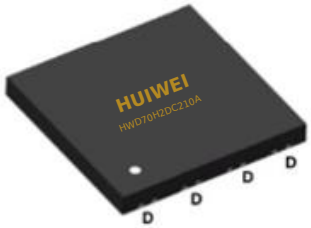
This is a 700V GaN-on-Si enhancement-mode power transistor in DFN8x8 package. The properties of GaN allow for high current, high breakdown voltage and high switching frequency. The DFN8x8 package offers low parasitic inductance, strong heat dissipation capability and high solderability, which make GaN better apply to consumer and industrial applications.

Features

- Ultra-low FOM
- Ultra-high switching frequency
- Reverse current capability
- Zero reverse recovery loss
- Monolithic integrated ESD protection
- RoHS, Pb-free, REACH-compliant

Applications

- AC/DC converters
- DC/DC converters
- Bridgeless totem pole PFC
- Fast chargers
- Power adapters
- LED lighting drivers
- Wireless power transfer
- Laser drivers
- TV display



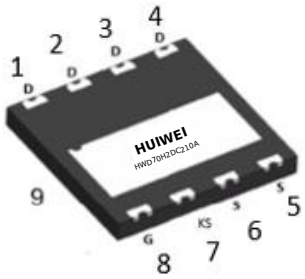


Table 1 Key Performance Parameters at T_j = 25 °C

Parameters	Values	Units
$V_{DS, max}$	700	V
$R_{DS(on), max}$	210	mΩ
Q_G	1.8	nC
$I_{D, Pulse}$	20	A
Q_{OSS} @ 400 V	15.5	nC
Q_{rr}	0	nC

Table 2 Pin Information

Gate	Drain	Kelvin Source	Source
8	1,2,3,4	7	5,6,9

Table3 Ordering Information

Ordering Code	Package	Product code
HWD70H2DC210A	DFN8*8	HWD70H2DC210A

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1 Maximum ratings

at T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime.

Table 3 Maximum rating

Parameters	Symbols	Values	Units	Notes/Test Conditions
Drain-source voltage	$V_{DS, max}$	700	V	V_{GS} = 0 V Tj = -55℃ to 150℃
Drain-source voltage transient [1]	$V_{DS, transient}$	800	V	V_{GS} = 0 V
Continuous current, drain-source	I_D	11	A	T_c = 25 °C
Pulsed current, drain-source [2]	$I_{D, pulse}$	20	A	T_c = 25 °C; V_G = 6 V
Pulsed current, drain-source [2]	$I_{D, pulse}$	11	A	T_c = 125 °C; V_G = 6 V
Gate-source voltage, continuous	V_{GS}	-6 to +7	V	T_j = -55 °C to 150 °C
Gate-source voltage, pulsed	$V_{GS, pulse}$	-20 to +10	V	T_j = -55 °C to 150 °C; t_{Pulse} = 50 ns, f = 100 kHz; open drain
Power dissipation	P_{tot}	57	W	T_c = 25 °C
Operating temperature	T_j	-55 to +150	°C	
Storage temperature	T_{stg}	-55 to +150	°C	

1. $V_{DS, transient}$ is intended for surge rating during non-repetitive events, t_{Pulse} < 1 µs.
2. Pulse width = 10 µs.

2 Thermal characteristics

Table 4 Thermal characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Thermal resistance, junction-ambient	R_{thJA}		80		°C/W	
Thermal resistance, junction-case	R_{thJC}	-	2.18	-	°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

3 Electrical characteristics

at T_j = 25 °C, unless specified otherwise.

Table 5 Static characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(TH)}$	1.1	1.4	2.5	V	I_D = 8.5 mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	1.45	-		I_D = 8.5 mA; V_{DS} = V_{GS}; T_j = 125 °C
Drain-source leakage current	I_{DSS}	-	0.1	24	μA	V_{DS} = 700 V; V_{GS} = 0 V; T_j = 25 °C
		-	2	-		V_{DS} = 700 V; V_{GS} = 0 V; T_j = 125 °C
Gate-source leakage current	I_{GSS}	-	40		μA	V_{GS} = 6 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	160	210	mΩ	V_{GS} = 6 V; I_D = 3 A; T_j = 25 °C
		-	370	-	mΩ	V_{GS} = 6 V; I_D = 3 A; T_j = 150 °C
Gate resistance	R_G	-	15	-	Ω	f = 5 MHz; open drain

Table 6 Dynamic characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	77	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100KHZ
Output capacitance	C_{oss}	-	20	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100KHZ
Reverse transfer capacitance	C_{rss}	-	0.14	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100KHZ
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	27.5	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	36.6	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output charge	Q_{OSS}	-	15.5	-	nC	V_{GS} = 0 V; V_{DS} = 0 to 400 V

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.
2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.

Table 7 Gate charge characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate charge	Q_G	-	1.8	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D = 3 A
Gate-source charge	Q_{GS}	-	0.18	-	nC	
Gate-drain charge	Q_{GD}	-	0.65	-	nC	
Gate plateau voltage	V_{plat}	-	2.1	-	V	V_{DS} = 400 V; I_D = 3 A

Table 8 Reverse conduction characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Source-drain reverse voltage	V_{SD}	-	3.5	-	V	V_{GS} = 0 V; I_{SD} = 3 A
Pulsed current, reverse	$I_{S,\ pulse}$	-	-	20	A	V_{GS} = 6 V
Reverse recovery charge [1]	Q_{rr}	-	0	-	nC	I_{SD} = 3A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

1. Excluding Q_{OSS}

4 Electrical characteristics diagrams

at T_j = 25 °C, unless specified otherwise.

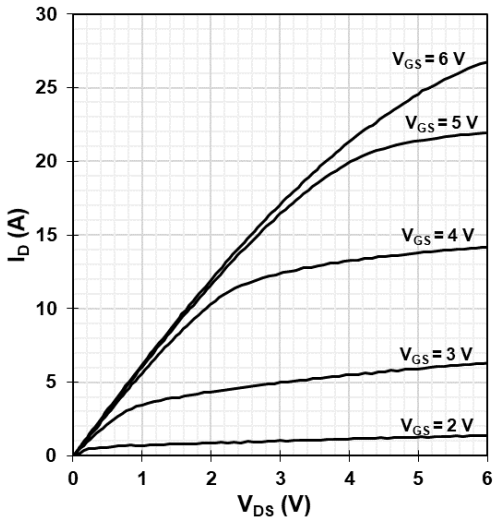
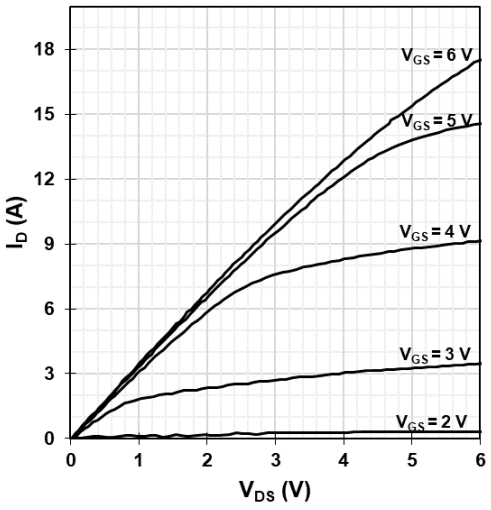
Figure 1 Typ. output characteristics	**Figure 2 Typ. output characteristics**
	
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C	$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

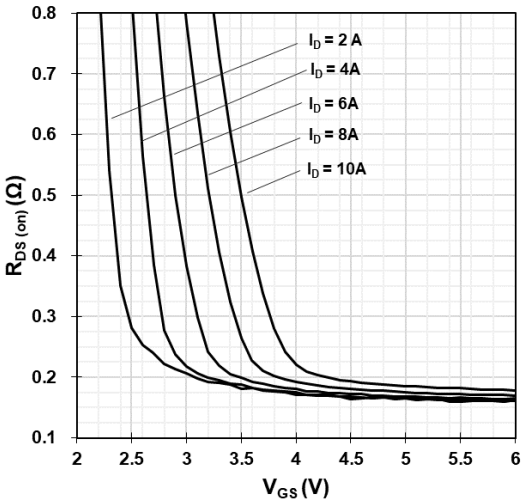
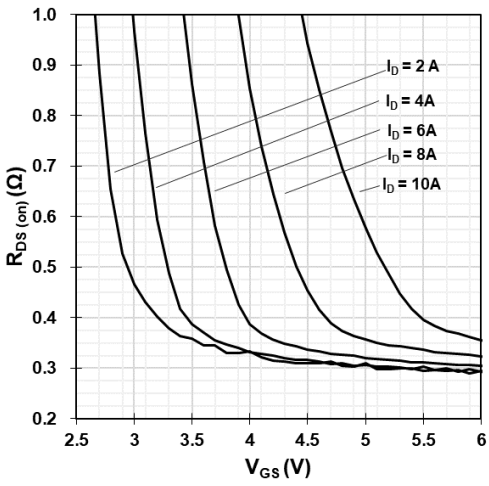
Figure 3 Typ. drain-source on-state resistance	**Figure 4 Typ. drain-source on-state resistance**
	
$R_{DS(on)} = f(I_D, V_{GS})$; T_j = 25 °C	$R_{DS(on)} = f(I_D, V_{GS})$; T_j = 125 °C

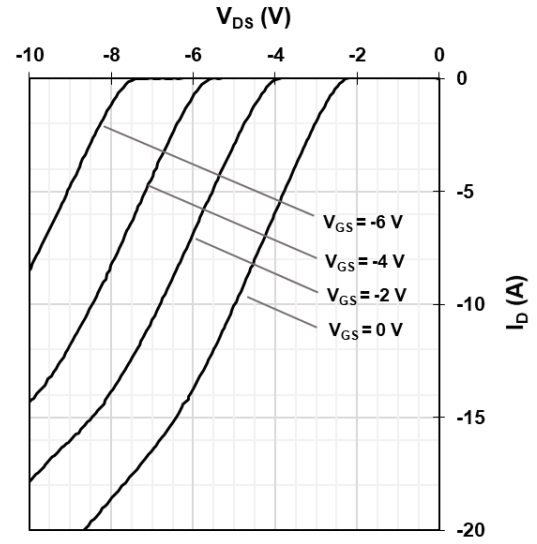
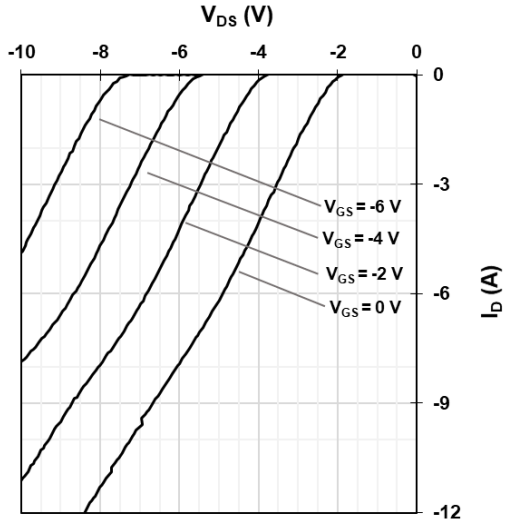
Figure 5 Typ. channel reverse characteristics	Figure 6 Typ. channel reverse characteristics
	
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C	$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

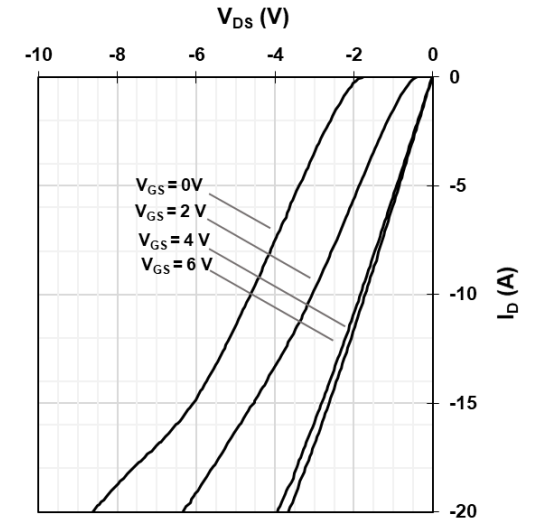
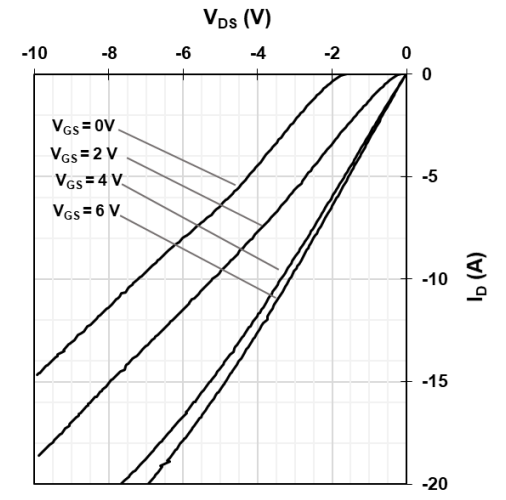
Figure 7 Typ. channel reverse characteristics	Figure 8 Typ. channel reverse characteristics
	
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C	$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

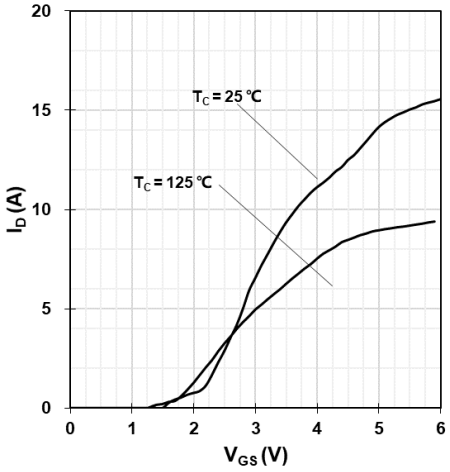
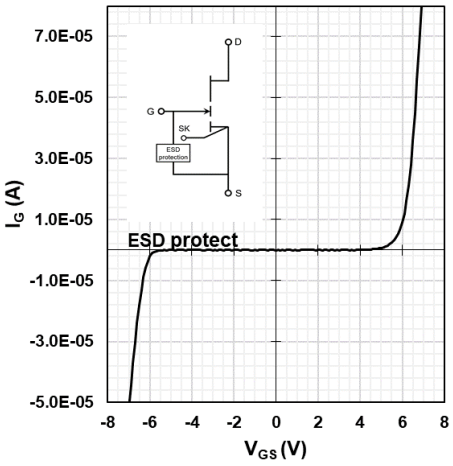
Figure 9 Typ. transfer characteristics	Figure 10 Typ. gate-to-source leakage
	
$I_D = f(V_{GS})$; V_{DS} = 3 V	$I_G = f(V_{GS})$; V_D = open

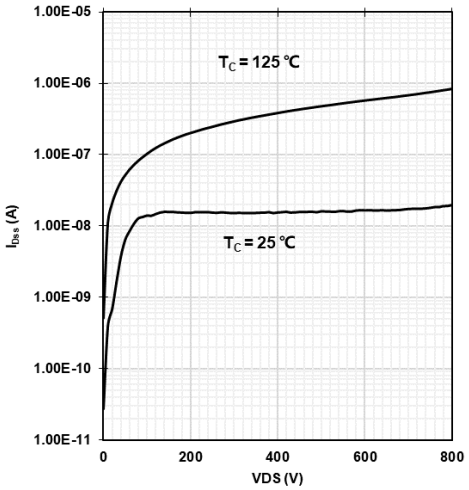
Figure 11 Drain-source leakage characteristics

Idss = f(Vds); Vgs = 0V

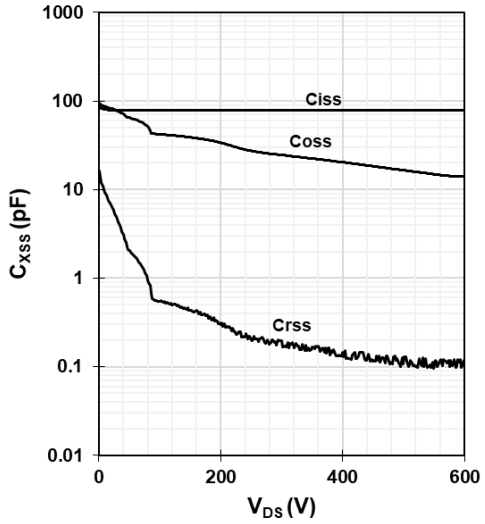
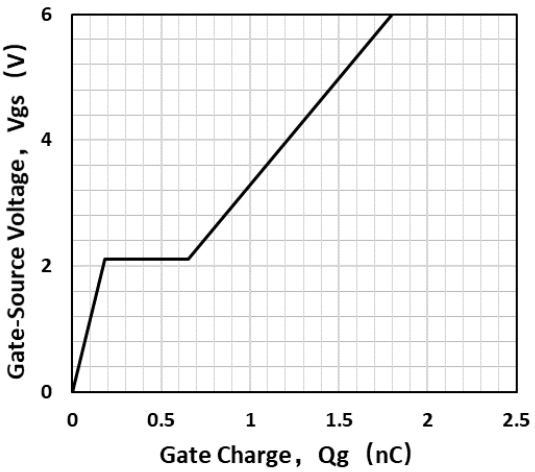
Figure 12 Typ. capacitances	Figure 13 Typ. gate charge
	
C_{XSS} = f(V_{DS}); Freq. = 100kHz	V_{GS} = f(Q_G); V_{DS} = 400 V; I_D = 3 A

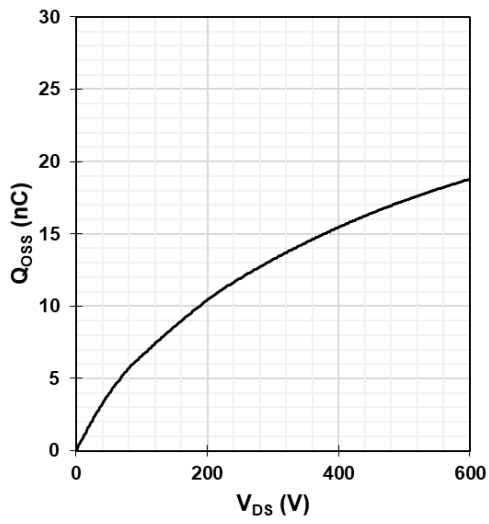
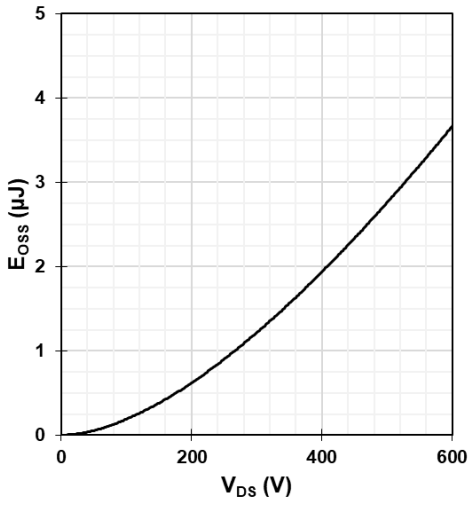
Figure 14 Typ. output charge	Figure 15 Typ. C_{oss} stored energy
	
Q_{OSS} = f(V_{DS}); Freq. = 100khz	E_{OSS} = f(V_{DS}); Freq. = 100khz

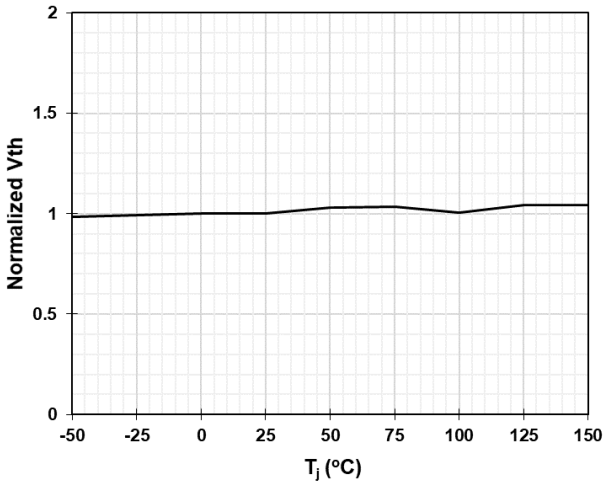
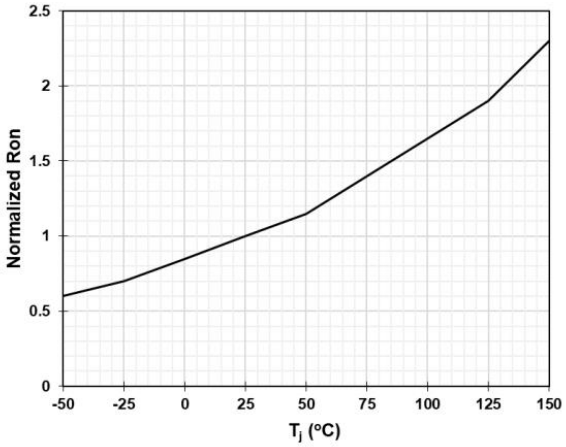
Figure 16 Gate threshold voltage	Figure 17 Drain-source on-state resistance
	
$V_{GS(TH)} = f(T_j)$; $V_{GS} = V_{DS}$; I_D = 8.5 mA	$R_{DS(on)} = f(T_j)$; I_D = 3A; V_{GS} = 6 V

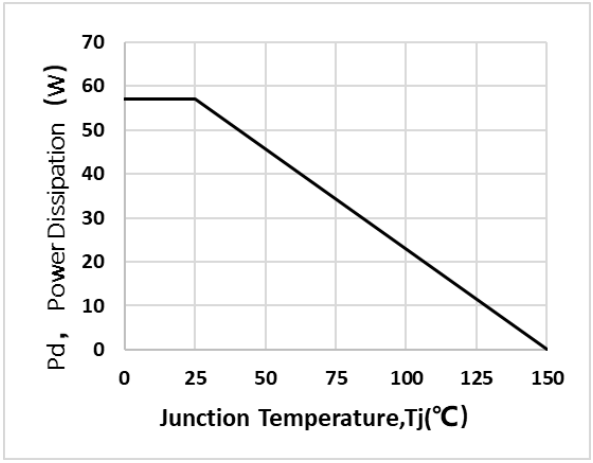
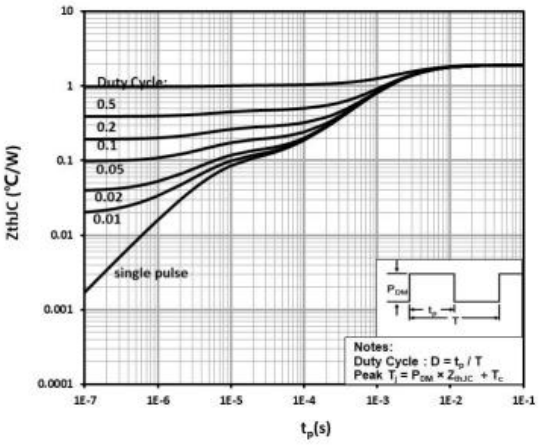
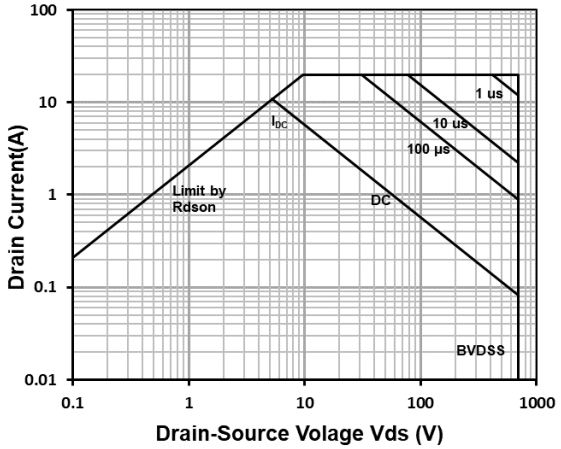
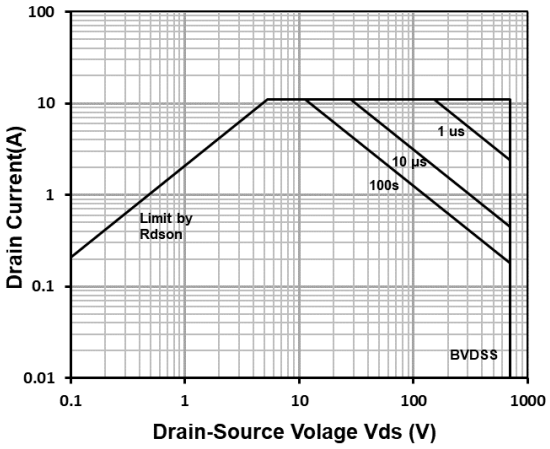
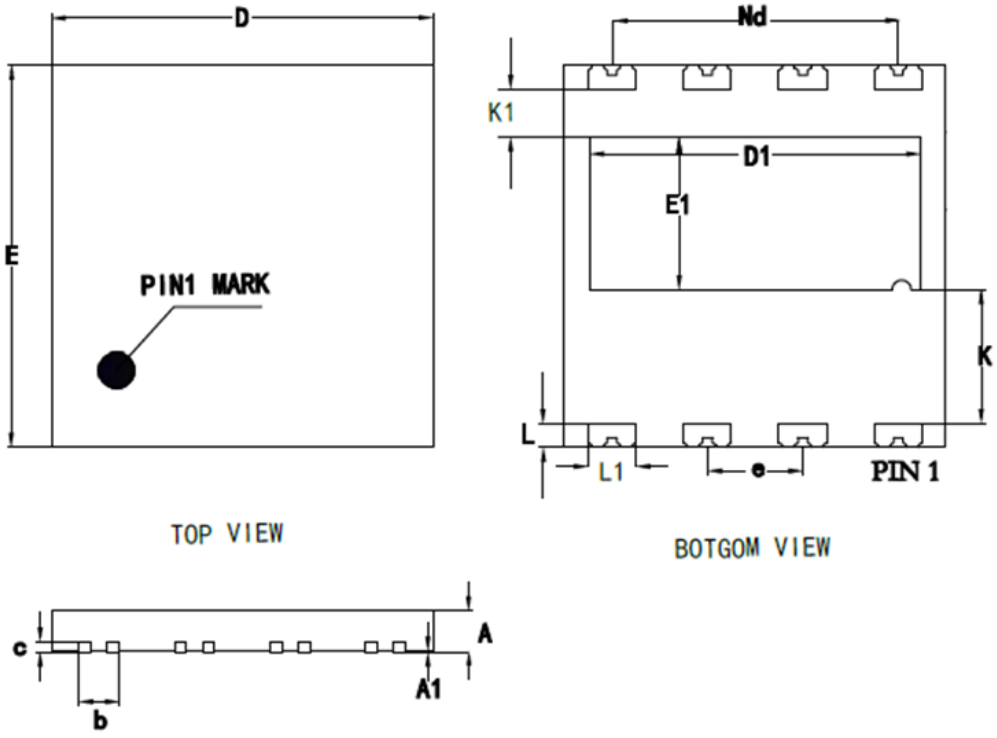
Figure 18 Power dissipation	Figure 19 Max.transient thermal impedance
	
Ptot = f(Tc)	Zthjc = f(tp,D)

Figure 20 Safe Operation Area	Figure 21 Safe Operation Area
	
Id = f(Vds); Tc = 25℃	Id = f(Vds); Tc = 125℃

5 Package outlines



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
C	—	0.203	—
b	0.80	0.85	0.90
D	7.90	8.00	8.10
D1	6.84	6.94	7.04
E	7.90	8.00	8.10
E1	3.40	3.20	3.60
e	2.00 BSC		
K	—	2.80	—
K1	0.90	1.00	1.10
L	0.490	0.50	0.51
L1	0.90	1.00	1.10
Nd	5.90	6.00	6.10

6 Revision history

Major changes since the last revision

Revision	Date	Description of changes
0.1	2026-07-03	0.1 version release
Ver1-1	2026-11-14	Centered HUIWEI / full part number marking; page-one title changed to the full HWD part number.