HWD10L1WL110B

RoHS COMPLIANT | Pb Pb-Free | HSF HALOGEN FREE

Description

This is a 100V GaN-on-Si enhancement-mode power transistor in WLCSP with 1.5mm x 1.5mm package size. The properties of GaN allow for high current, high breakdown voltage and high switching frequency.

Features

- Higher switching frequency
- Lower switching losses and lower driver power
- Lower conduction
- Zero reverse recovery loss
- RoHS, Pb-free, REACH-compliant

Applications

- Automotive lidar/TOF
- 48V servers
- Pulsed power
- Isolated power supplies
- Point of load converters
- Class D audio
- LED lighting
- Low inductance motor drive

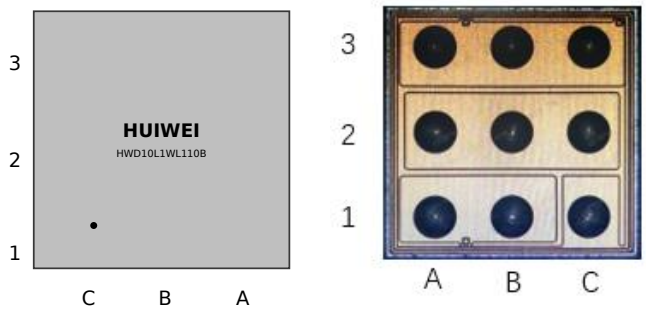


Table 1 Key Performance Parameters at T_j = 25 °C

Parameters	Values	Units
$V_{DS,\ max}$	100	V
$R_{DS(on),\ max}$	11	mΩ
Q_G, typ@V_{DS}=50V	2.1	nC
$I_{D,\ Pulse}$	100	A
Q_{OSS} @ 50 V	9.5	nC

Table 2 Pin Information

Gate	Drain	Source
C1	A2,B2,C2	A1,B1,A3,B3,C3

Table3 Ordering Information

Ordering Code	Package	Product code
HWD10L1WL110B	WLCSP	HWD10L1WL110B

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1 Maximum ratings

at T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime.

Table 4 Maximum rating

Parameters	Symbols	Values	Units	Notes/Test Conditions
Drain-to-source voltage(Continuous)	V_{DS}	100	V	V_{GS} = 0 V
Continuous current, drain-source	I_D	27	A	T_B = 25 °C
Continuous current, drain-source	I_D	12	A	T_B = 100 °C
Pulsed current, drain-source [1]	$I_{D, pulse}$	100	A	T_c = 25 °C; V_G = 5V
Pulsed current, drain-source [1]	$I_{D, pulse}$	80	A	T_c = 125 °C; V_G = 5V
Gate-source voltage, continuous	V_{GS}	-4 to +6	V	
Operating temperature	T_j	-40 to +150	°C	
Storage temperature	T_{stg}	-55 to +150	°C	

1. Pulse width = 10 μs.

2 Thermal characteristics

Table 5 Thermal characteristics

Parameters	Symbols	Values			Units
		Min.	Typ.	Max.	
Thermal resistance, junction to case (Case top)	R_{thJC}	-	1.6	-	°C/W
Thermal resistance, junction to Board (Case Bottom)	R_{thJB}	-	8	-	°C/W
Thermal resistance, junction to Ambient	R_{thJA}	-	95		
Reflow soldering temperature(MSL3)	T_{sold}	-	-	260	°C

3 Electrical characteristics

at T_j = 25 °C, unless specified otherwise.

Table 6 Static characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Drain to Source Voltage	BV_{DSS}	100	-	-	V	V_{GS}=0V
Gate threshold voltage	$V_{GS(TH)}$	0.7	1.4	2.5	V	I_D = 2.5 mA; V_{DS} = V_{GS}
Drain-source leakage	I_{DSS}	-	10	200	μA	V_{DS} = 100 V; V_{GS} = 0 V
Gate-to-source Forward leakage	I_{GSS}	-	10	500	μA	V_{GS} = 6 V; V_{DS} = 0 V
Gate-to-source Reverse leakage		-	0.01	0.1	μA	V_{GS} = -4 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	8	11	mΩ	V_{GS} = 5 V; I_D = 11 A
Source-Drain Forward Voltage	Vsd	-	1.8	-	V	I_S = 0.5A,V_{GS}=0V

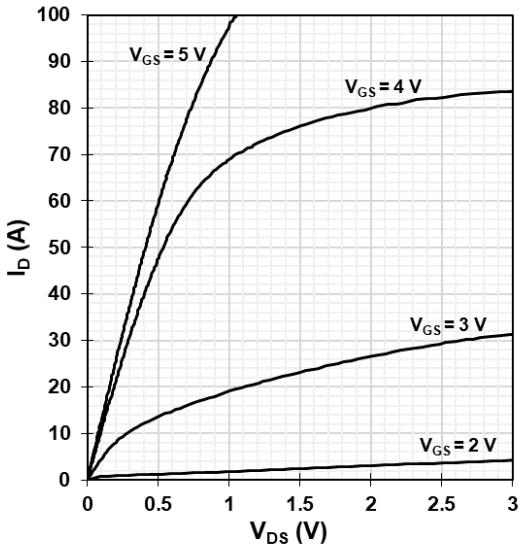
Table 7 Dynamic characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	233	-	pF	V_{GS} = 0 V; V_{DS} = 50 V; f = 100KHZ
Output capacitance	C_{oss}	-	128	-	pF	V_{GS} = 0 V; V_{DS} = 50 V; f = 100KHZ
Reverse transfer capacitance	C_{rss}	-	6.8	-	pF	V_{GS} = 0 V; V_{DS} = 50 V; f = 100KHZ

4 Electrical characteristics diagrams

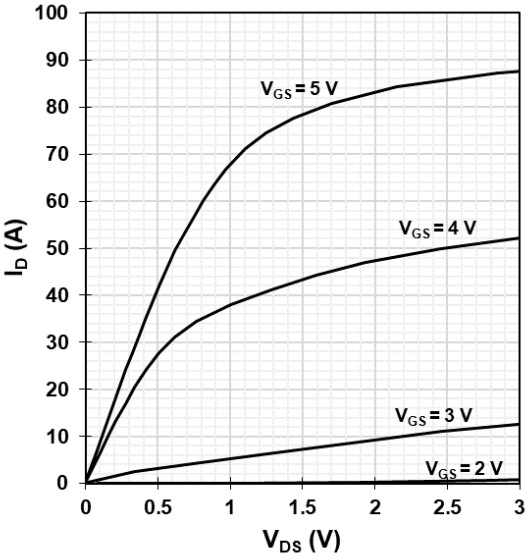
at T_j = 25 °C, unless specified otherwise.

Figure 1 Typ. output characteristics



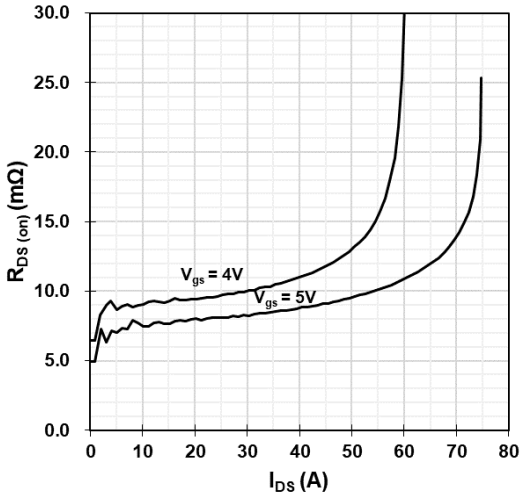
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C

Figure 2 Typ. output characteristics



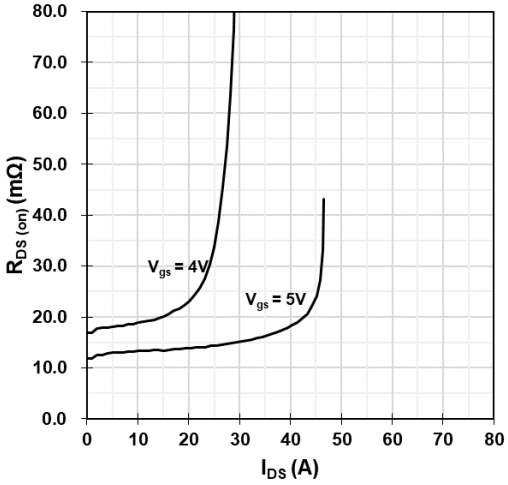
$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

Figure 3 Typ. drain-source on-state resistance



$R_{DS(on)} = f(V_{GS}, I_D)$; T_j = 25 °C

Figure 4 Typ. drain-source on-state resistance



$R_{DS(on)} = f(V_{GS}, I_D)$; T_j = 125 °C

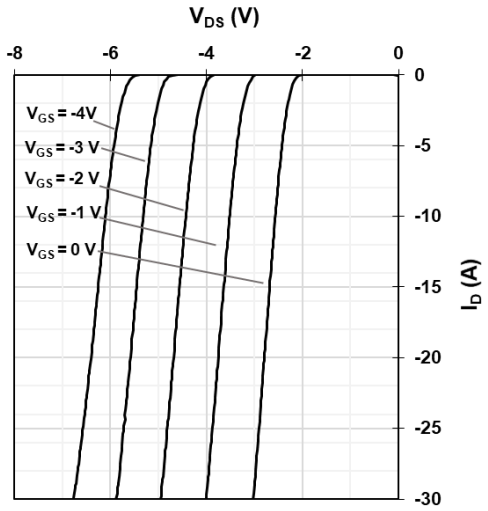
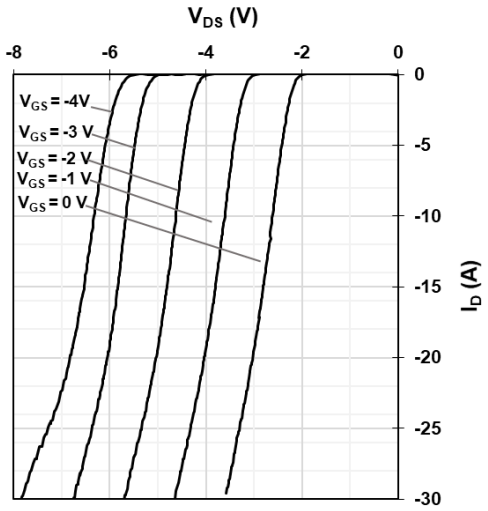
Figure 5 Typ. channel reverse characteristics	Figure 6 Typ. channel reverse characteristics
	
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C	$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

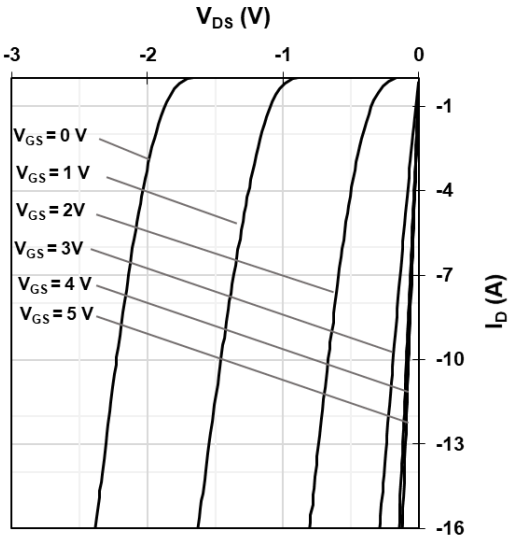
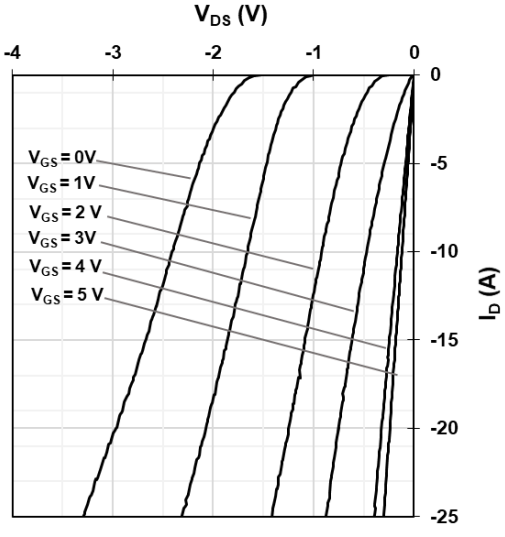
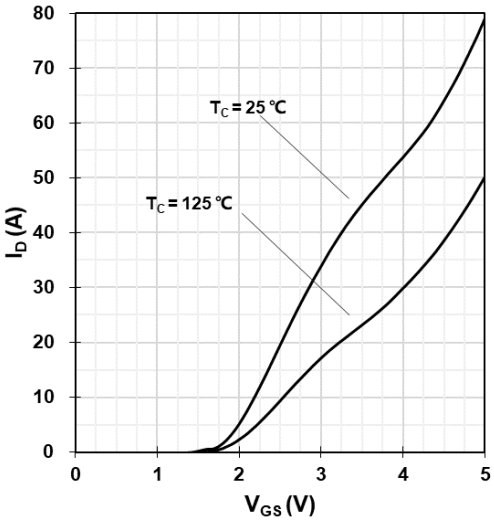
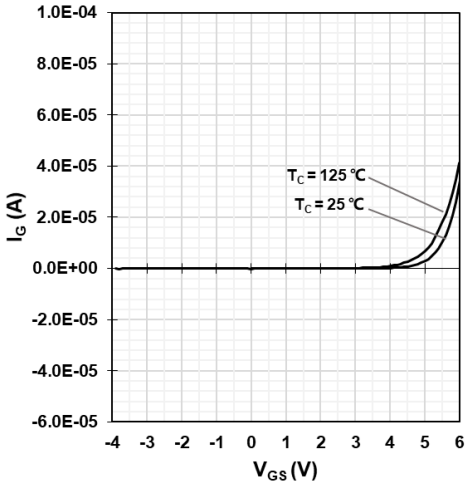
Figure 7 Typ. channel reverse characteristics	Figure 8 Typ. channel reverse characteristics
	
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C	$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

Figure 9 Typ. transfer characteristics



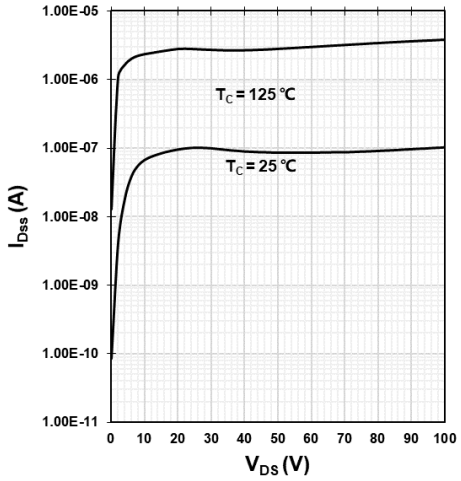
$I_D = f(V_{GS})$; V_{DS} = 3 V

Figure 10 Typ. gate-to-source leakage



$I_G = f(V_{GS})$; V_D = open

Figure 11 Drain-source leakage characteristics



Idss = f(Vds); Vgs = 0V

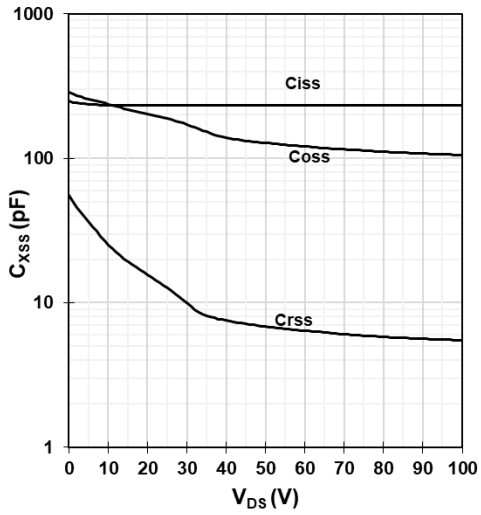
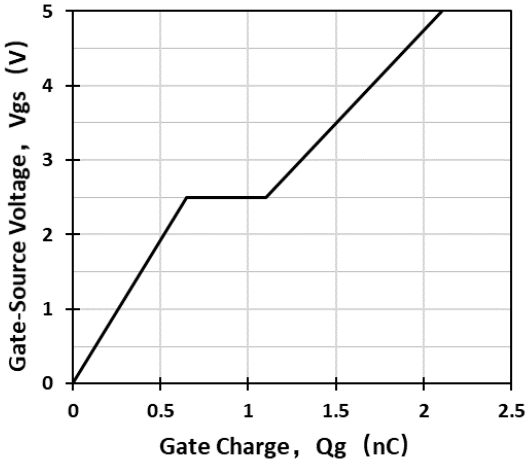
Figure 12 Typ. capacitances	Figure 13 Typ. gate charge
	
C_{XSS} = f(V_{DS}); Freq. = 100kHz	V_{GS} = f(Q_G); V_{DS} = 50 V; I_D = 11A

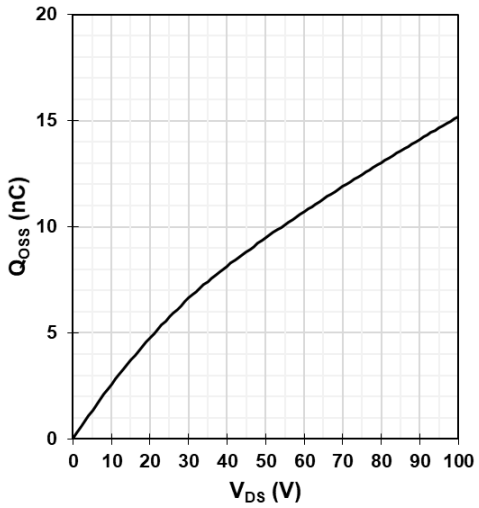
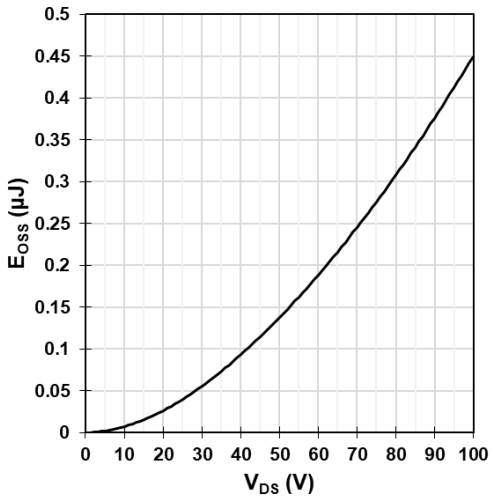
Figure 14 Typ. output charge	Figure 15 Typ. C_{oss} stored energy
	
Q_{OSS} = f(V_{DS}); Freq. = 100khz	E_{OSS} = f(V_{DS}); Freq. = 100khz

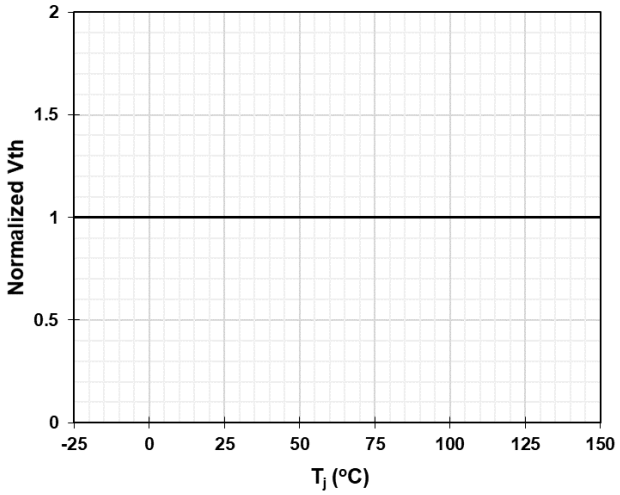
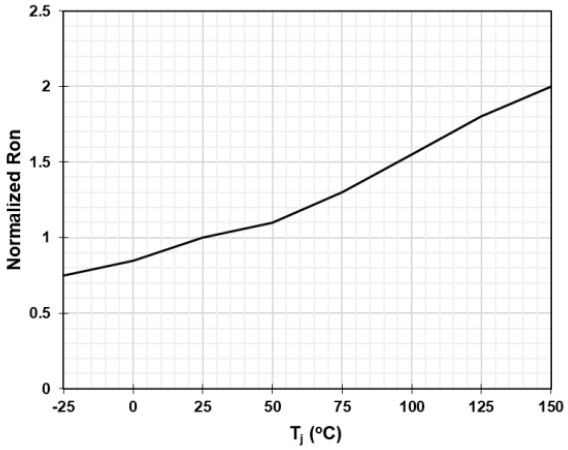
Figure 16 Gate threshold voltage	Figure 17 Drain-source on-state resistance
	
$V_{GS(TH)} = f(T_j)$; $V_{GS} = V_{DS}$; I_D = 2.5 mA	$R_{DS(on)} = f(T_j)$; I_D = 11 A; V_{GS} = 5 V

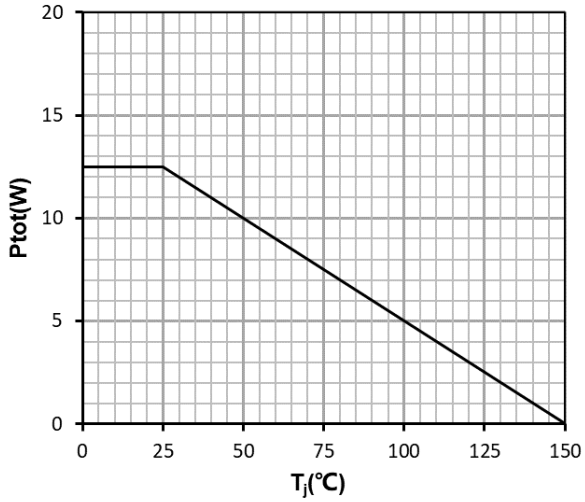
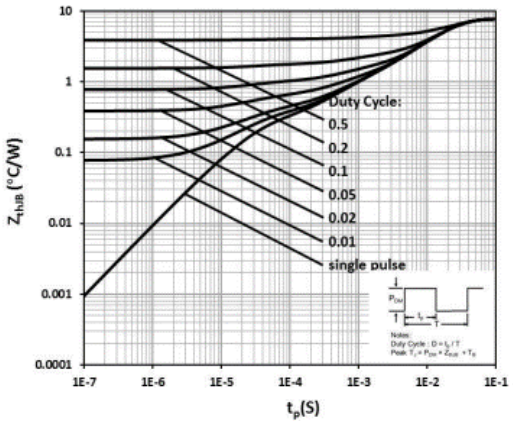
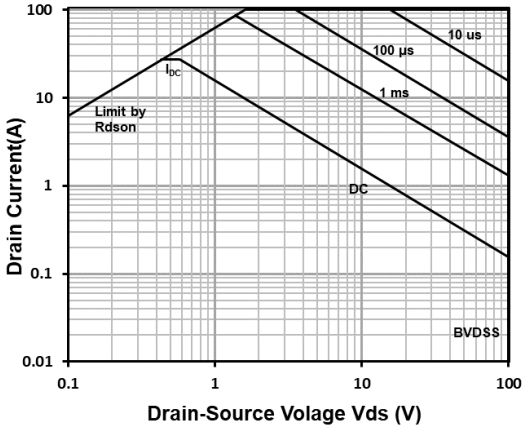
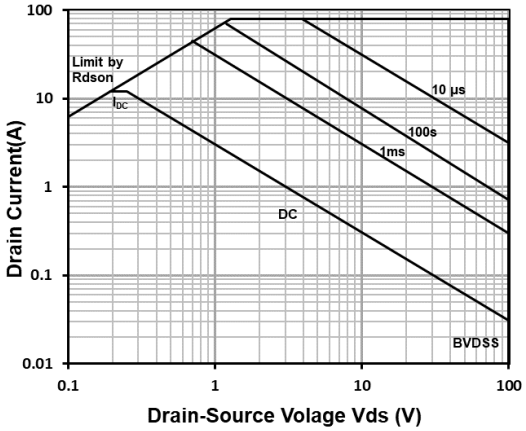
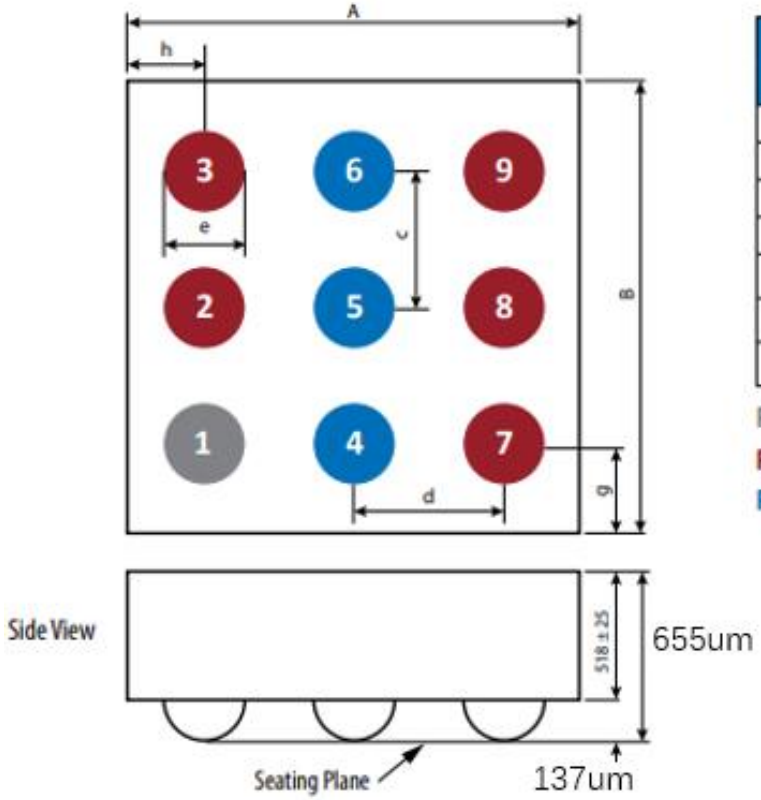
Figure 18 Power dissipation	Figure 19 Max.transient thermal impedance
	
Ptot = f(Tc)， $R_{\theta JB}$ = 8 ˚C/W	Zthjb = f(tp,D)

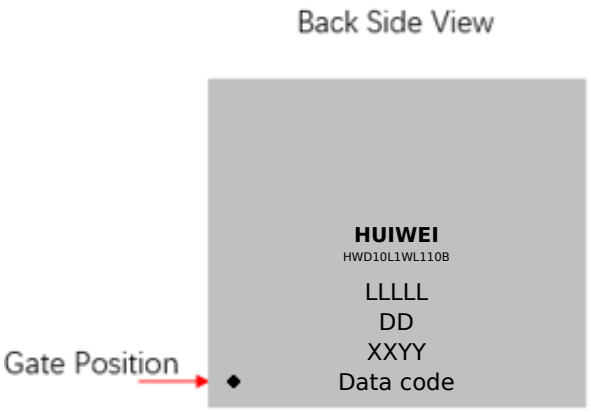
Figure 20 Safe Operation Area	Figure 21 Safe Operation Area
	
Id = f(Vds); Tc = 25℃	Id = f(Vds); Tc = 125℃

5 Package outlines



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	1470	1500	1530
B	1470	1500	1530
c		450	
d		500	
e		250	
g		300	
h		250	

Pad 1 is Gate;
Pads 2, 3, 7, 8, 9 are Source;
Pads 4, 5, 6 are Drain



行数	Marking
1	Product
2	LOT ID
3	Wafer ID
3	Die Coordinate
4	Data code
5	PIN1

6 Revision history

Major changes since the last revision

Revision	Date	Description of changes
0.1	2026-05-23	0.1 version release
Ver1-1	2026-11-14	Centered HUIWEI / full part number marking; page-one title changed to the full HWD part number.