HWD10L1FQ025A

RoHS COMPLIANT | Pb Pb-Free | HSF HALOGEN FREE

Description

This is a 100V GaN-on-Si enhancement-mode power transistor in FCQFN with 5mm*3mm package size. The properties of GaN allow for high current, high breakdown voltage and high switching frequency.

Features

- Higher switching frequency
- Lower switching losses and lower driver power
- Lower conduction
- Zero reverse recovery loss
- RoHS, Pb-free, REACH-compliant

Applications

- High frequency DC-DC converter
- BMS protection
- RF envelope tracking
- PC charger
- Mobile power bank
- Motor driver

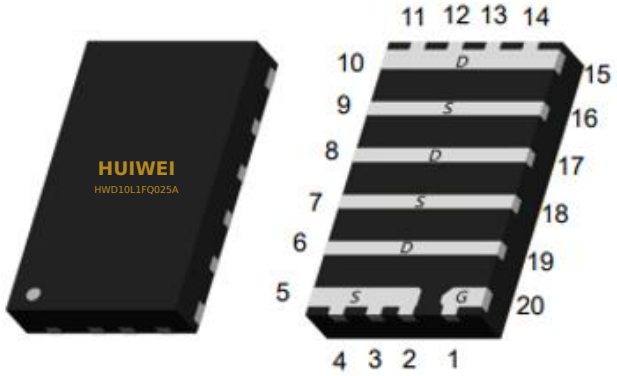


Table 1 Key Performance Parameters at T_j = 25 °C

Parameters	Values	Units
$V_{DS,\ max}$	100	V
$R_{DS(on),\ max}$@V_{GS}=5V	2.5	mΩ
$Q_{G,\ typ}$@V_{DS}=50V	12.5	nC
$I_{D,\ Pulse}$	320	A
Q_{OSS} @ 50 V	56	nC

Table 2 Pin Information

Gate	Drain	Source
1,20	6,8,10-15,17,19	2-5,7,9,16,18

Table3 Ordering Information

Ordering Code	Package	Product code
HWD10L1FQ025A	FCQFN3*5	HWD10L1FQ025A

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1 Maximum ratings

at T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime.

Table 4 Maximum rating

Parameters	Symbols	Values	Units	Notes/Test Conditions
Drain-to-source voltage(Continuous)	V_{DS}	100	V	V_{GS} = 0 V
Continuous current, drain-source	I_D	80	A	T_c = 25 °C
Pulsed current, drain-source [1]	$I_{D, pulse}$	320	A	T_c = 25 °C; V_G = 5V
Gate-source voltage, continuous	V_{GS}	-4 to +6	V	
Operating temperature	T_j	-40 to +150	°C	
Storage temperature	T_{stg}	-40 to +150	°C	

1. Pulse width = 100 μs.

2 Thermal characteristics

Table 5 Thermal characteristics

Parameters	Symbols	Values			Units
		Min.	Typ.	Max.	
Thermal resistance, junction to case (Case top)	R_{thJC}	-	14.2	-	°C/W
Thermal resistance, junction to Board (Case Bottom)	R_{thJB}	-	1.9	-	°C/W
Thermal resistance, junction to Ambient	R_{thJA}	-	61		°C/W
Reflow soldering temperature(MSL3)	T_{sold}	-	260	-	°C

3 Electrical characteristics

at T_j = 25 °C, unless specified otherwise.

Table 6 Static characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Drain to Source Voltage	BV_{DSS}	100	-	-	V	V_{GS}=0V
Gate threshold voltage	$V_{GS(TH)}$	0.8	1.3	2.5	V	I_D = 10 mA; V_{DS} = V_{GS}
Drain-source leakage	I_{DSS}	-	10	200	μA	V_{DS} = 100 V; V_{GS} = 0 V
Gate-to-source Forward leakage	I_{GSS}	-	20	200	μA	V_{GS} = 6 V; V_{DS} = 0 V
Gate-to-source Reverse leakage		-	0.01	0.5	μA	V_{GS} = -4 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	1.9	2.5	mΩ	V_{GS} = 5 V; I_D = 30A
Source-Drain Forward Voltage	Vsd	-	2.0	-	V	I_S = 0.5A,V_{GS}=0V

Table 7 Dynamic characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1305	-	pF	V_{GS} = 0 V; V_{DS} = 50 V; f = 100KHZ
Output capacitance	C_{oss}	-	695	-	pF	V_{GS} = 0 V; V_{DS} = 50 V; f = 100KHZ
Reverse transfer capacitance	C_{rss}	-	26.4	-	pF	V_{GS} = 0 V; V_{DS} = 50 V; f = 100KHZ
Total Gate Charge	Q_G	-	12.5	-	nC	V_{GS} = 5 V, V_{DS} = 0 V to 50 V, I_D= 30 A
Gate to Source Charge	Q_{GS}	-	2.8	-		V_{GS} = 5 V, V_{DS} = 0 V to 50 V, I_D= 30 A
Gate to Drain Charge	Q_{GD}	-	3.5	-		V_{GS} = 5 V, V_{DS} = 0 V to 50 V, I_D= 30 A
Gate Plateau Voltage	V_{Plat}	-	2	-	V	I_D = 30 A, V_{DS} = 50 V, V_{GS} = 0 V to 5 V
Output Charge	Q_{OSS}	-	56	-	nC	V_{GS} = 0 V, V_{DS} = 0 V to 50 V
Reverse recovery charge	Q_{RR}	-	0	-		V_{DS} = 50 V, I_S = 30 A

4 Electrical characteristics diagrams

at T_j = 25 °C, unless specified otherwise.

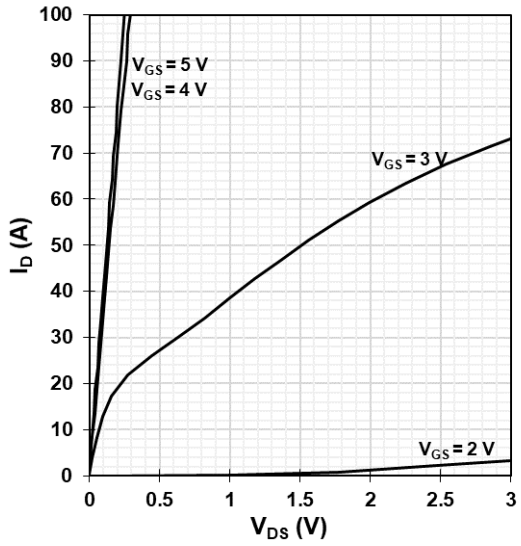
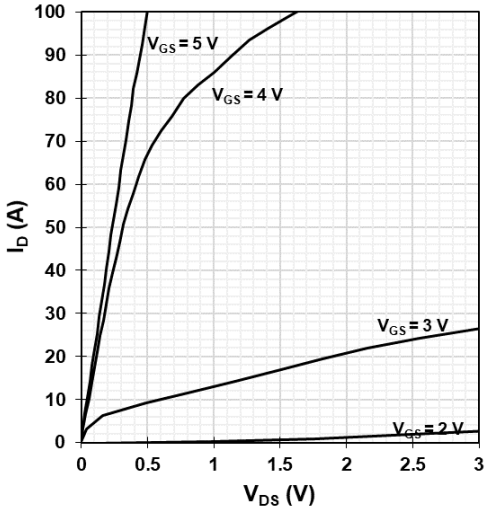
Figure 1 Typ. output characteristics	**Figure 2 Typ. output characteristics**
	
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C	$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

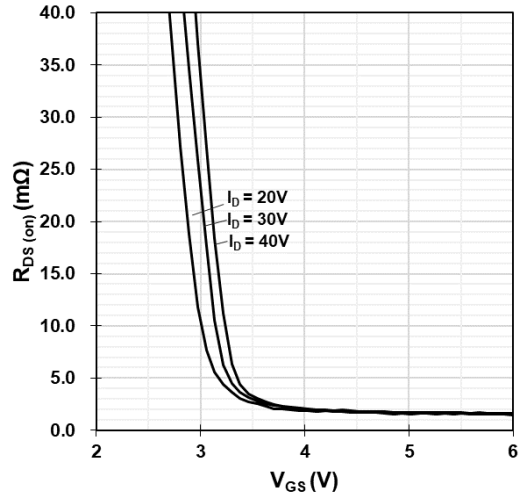
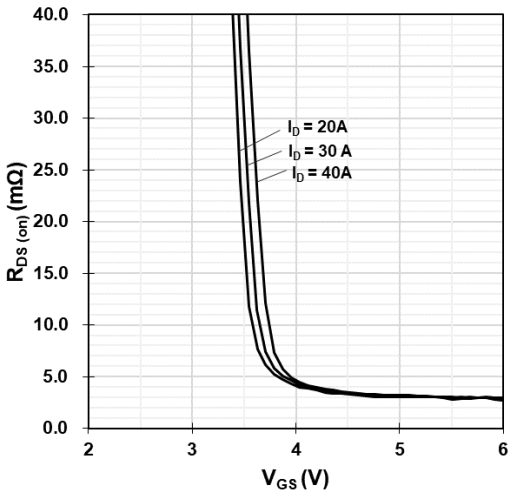
Figure 3 Typ. drain-source on-state resistance	**Figure 4 Typ. drain-source on-state resistance**
	
$R_{DS(on)} = f(V_{GS}, I_D)$; T_j = 25 °C	$R_{DS(on)} = f(V_{GS}, I_D)$; T_j = 125 °C

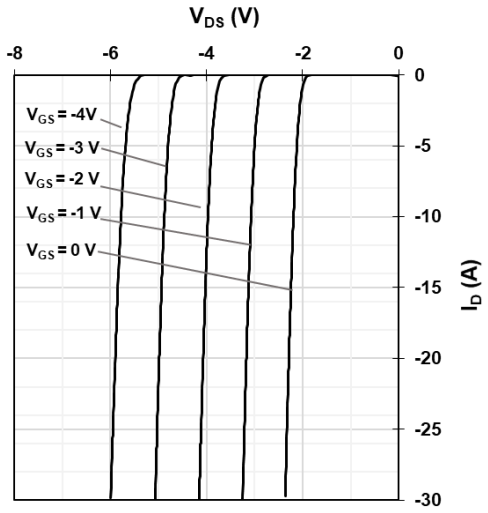
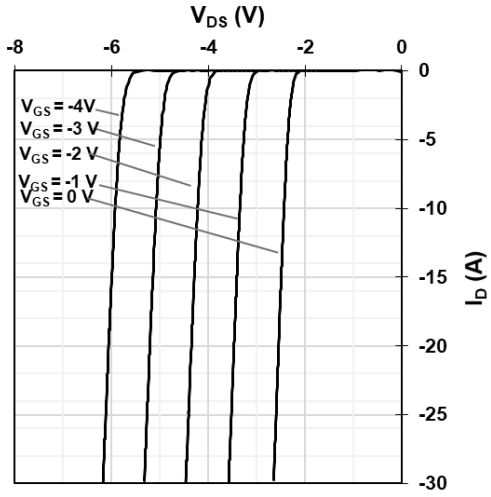
Figure 5 Typ. channel reverse characteristics	Figure 6 Typ. channel reverse characteristics
	
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C	$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

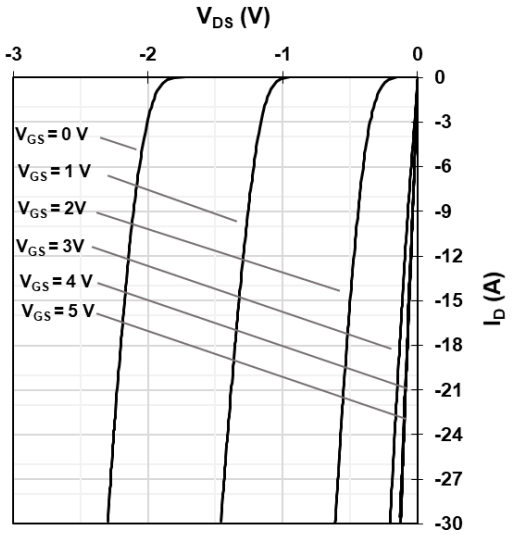
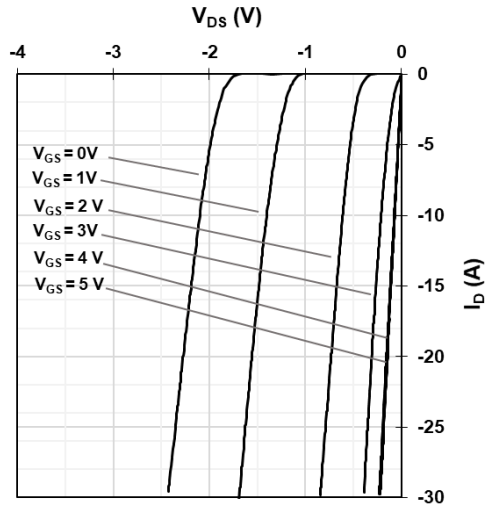
Figure 7 Typ. channel reverse characteristics	Figure 8 Typ. channel reverse characteristics
	
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C	$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

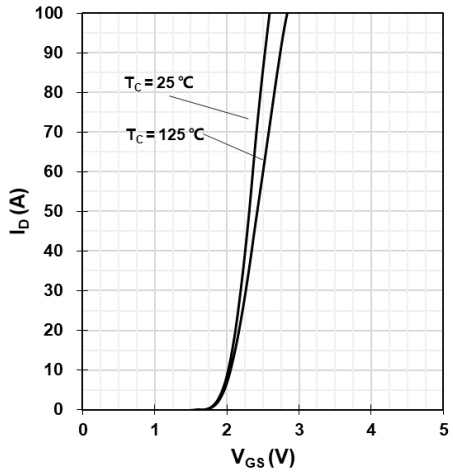
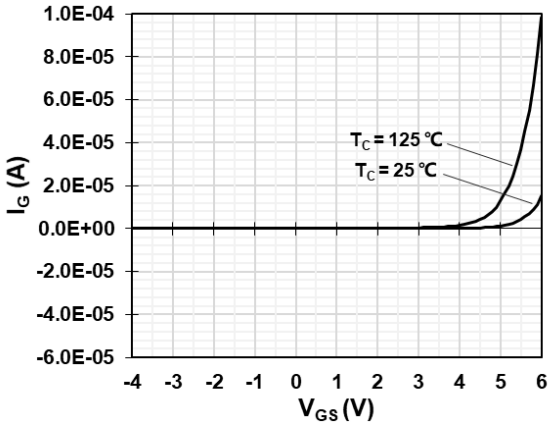
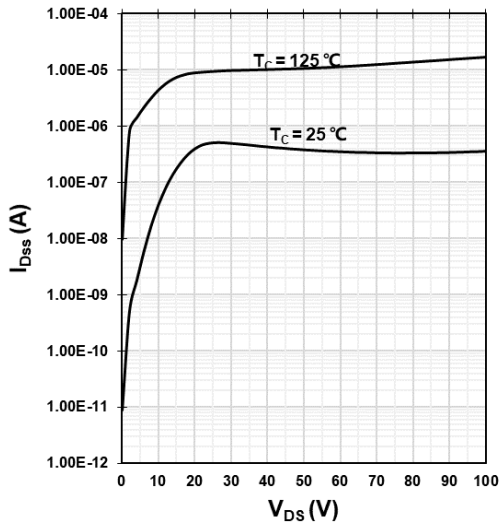
Figure 9 Typ. transfer characteristics	Figure 10 Typ. gate-to-source leakage
	
$I_D = f(V_{GS})$; V_{DS} = 3 V	$I_G = f(V_{GS})$; V_D = open

Figure 11 Drain-source leakage characteristics



Idss = f(Vds); Vgs = 0V

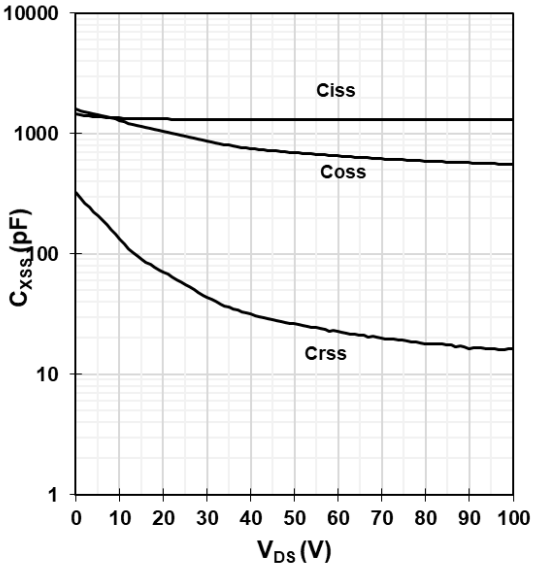
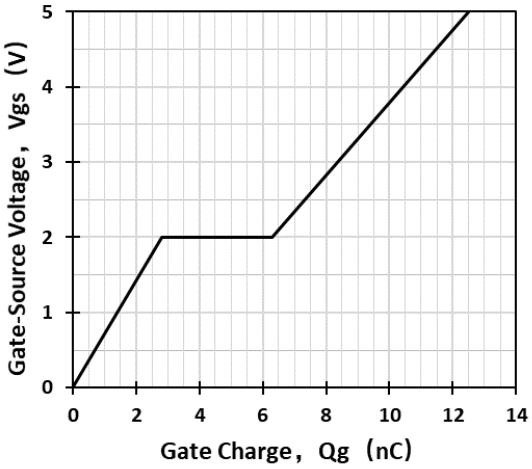
Figure 12 Typ. capacitances	Figure 13 Typ. gate charge
	
C_{XSS} = f(V_{DS}); Freq. = 100kHz	V_{GS} = f(Q_G); V_{DS} = 50 V; I_D = 30A

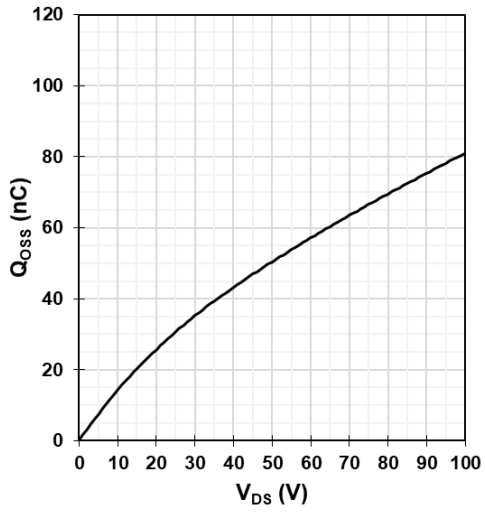
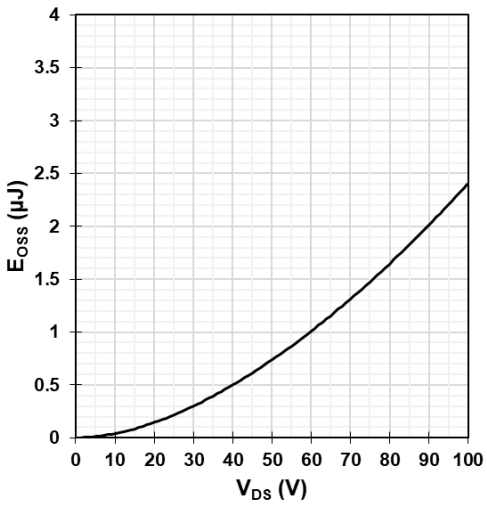
Figure 14 Typ. output charge	Figure 15 Typ. C_{oss} stored energy
	
Q_{OSS} = f(V_{DS}); Freq. = 100khz	E_{OSS} = f(V_{DS}); Freq. = 100khz

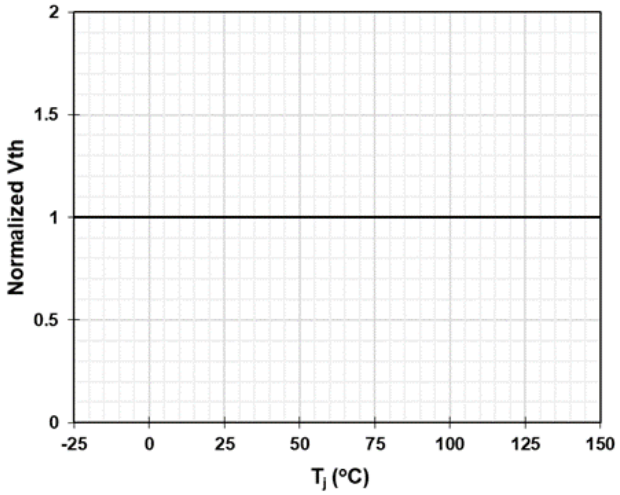
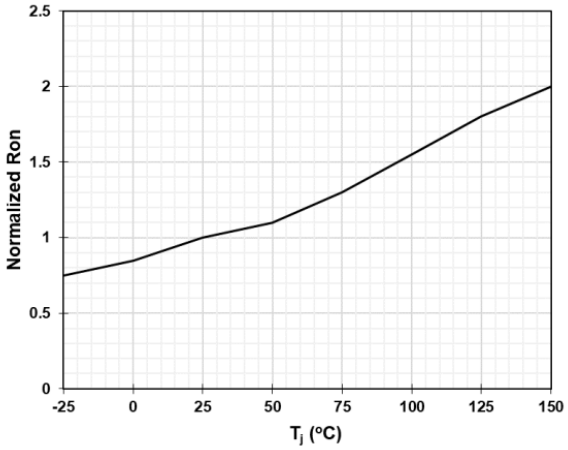
Figure 16 Gate threshold voltage	Figure 17 Drain-source on-state resistance
	
$V_{GS(TH)} = f(T_j)$; $V_{GS} = V_{DS}$; I_D = 10 mA	$R_{DS(on)} = f(T_j)$; I_D = 30 A; V_{GS} = 5 V

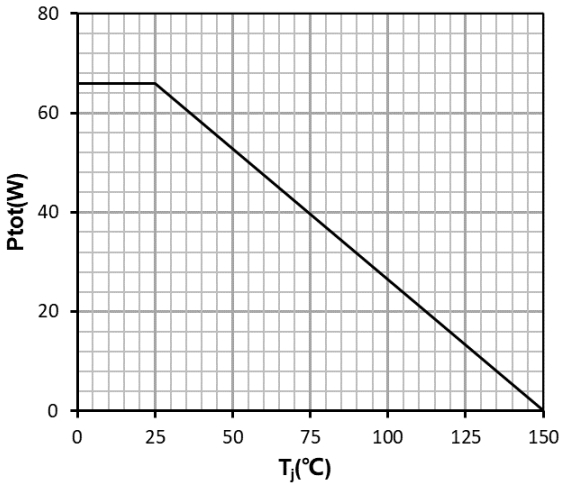
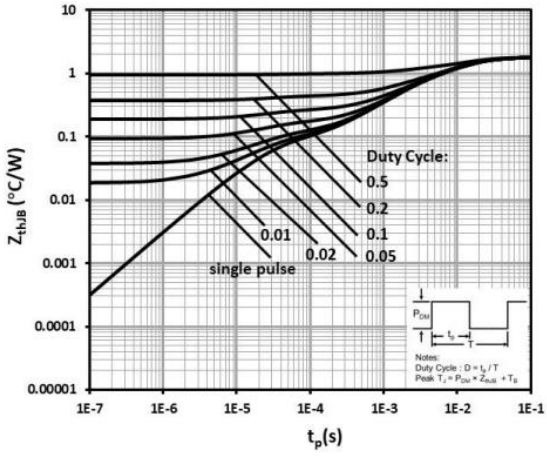
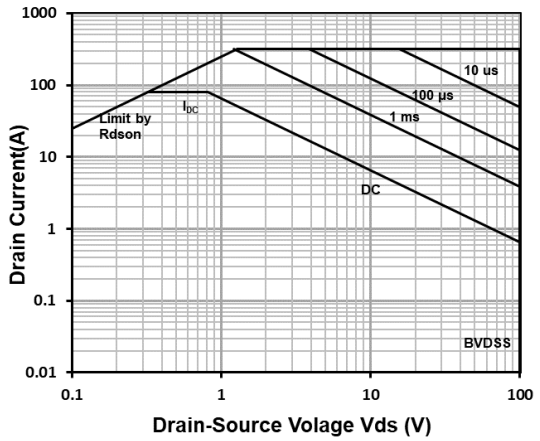
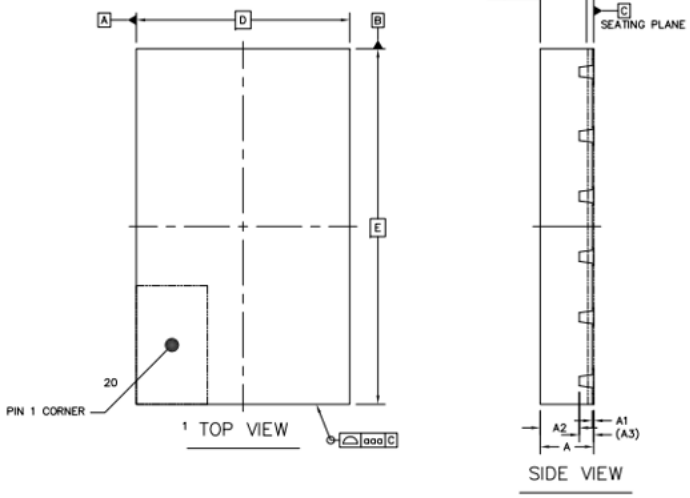
Figure 18 Power dissipation	Figure 19 Max.transient thermal impedance
	
Ptot = f(Tc)， $R_{\theta JB}$ = 8 ˚C/W	Zthjb = f(tp,D)

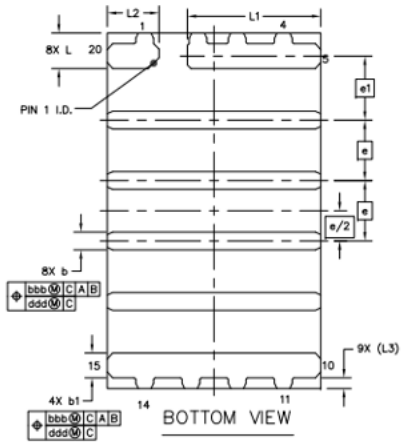
Figure 20 Safe Operation Area



Id = f(Vds); Tc = 25℃

5 Package outlines





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
		b1	0.3	0.35	0.4
BODY SIZE	X	D		3 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.85 BSC	
		e1		0.9 BSC	
LEAD LENGTH		L	0.4	0.5	0.6
		L1	1.775	1.875	1.975
		L2	0.625	0.725	0.825
LEAD EDGE TO PKG EDGE		L3		0.15 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	

6 Revision history

Major changes since the last revision

Revision	Date	Description of changes
0.1	2026-06-12	0.1 version release
Ver1-1	2026-11-14	Centered HUIWEI / full part number marking; page-one title changed to the full HWD part number.